Symposium I: Front-end junction and contact formation in future Silicon/Germanium based devices

This is one of three linked symposia at the European Materials Research Society 2008 Spring Meeting (symposia I, J and K) dealing with future CMOS technologies and silicon materials. This symposium will provide an open forum for the presentation of original experimental and theoretical studies that can contribute to the physical understanding of the various phenomena related to the implementation and optimisation of new materials and processes for future Silicon Based Devices. In particular, it will focus on specific issues concerning the fabrication of strain engineered substrates, ultra-shallow junctions and silicide/germanide contacts.

The improvement of the device performances has mainly relied on the continuous decrease of the MOS dimensions. During the last three decades, this miniaturisation has been assured by a "conservative" approach aiming at pursuing the use of well established process technologies (e.g. reduction of the implant energy for the junctions and of the oxide thickness for the gate stack). However, as the physical limits of conventional technologies are being reached, new and ever more complex phenomena are observed, that require a large amount of dedicated experimental and theoretical studies. For example, the defect-dopant interaction that limits the reduction of the S/D junction depth has generated extensive research on diffusion anomalies, defect engineering and alternative thermal processes. In addition, it is possible that the requirements of the future technology nodes will not be met by these efforts and the introduction of new structures and materials will be required to improve carrier mobility (strained Si and SiGe) and limit parasitic effects (SOI). Indeed, it is expected that both material types will be combined into a single process (SSOI) to further improve the device performances. This implies that, in addition to the materials fabrication and integration issues, all the previously mentioned phenomena (extensively studied in bulk Si) must be understood and controlled within these new materials, in particular taking into account strain and interface effects.

This symposium intends to bring together scientists and industrials to share experimental results, physical models and new ideas in this "fast-growing" research area. A general opening session of invited talks will be held jointly with the other two linked symposia. In addition, issues associated with the formation of ultra-shallow junctions in Ge and Ge-rich SiGe will be discussed in a joint session with symposium J (Beyond silicon technology: materials and devices for post-Si CMOS).

The symposium will include, but will not be limited to, the following topics:
• Silicon and new materials (including SiGe(C), Si:C, Ge and strained Si on bulk Si, SiGe virtual substrates and SOI), processes (growth and annealing), and characterization
• Advanced dopant incorporation methods (ion implantation, plasma-immersion implantation, in-situ doping and other methods)
• Thermal process modules for ultra-shallow junctions (Solid Phase Epitaxial Regrowth, high ramp-rate RTA, laser and flash anneals…)
• Metallic junctions for SBFET (formation and characterisation of silicides with low barrier height, dopant segregation technique, SBFET device fabrication and characterisation)
• Silicide and germanide formation, including characterization (phase formation and morphology, growth kinetics, mechanical stress, thermal stability, contact resistance, formation of silicide contacts to SiGe and Si:C…)
• Structural and electrical characterisation of defects (TEM, SIMS, 4PP, Hall, SRP, SCM and other methods)
• Surface and interface interactions with point defects and dopants (point-defects injection and annihilation, dopant outdiffusion, interdiffusion and segregation at the Si/SiGe or oxide interfaces…)
• Dopant diffusion and activation (dopant-defect interaction, defect evolution, strain effects, clustering/deactivation, transient diffusion mechanisms, diffusion in a-Si…)
• Defect engineering (point-defect injection, vacancy generation by high-energy implants, impurity co-implantation)
• Simulation and modelling of the above listed effects (from ab-initio to continuum TCAD)

Invited speakers:
Y. Cho (Applied Materials), C. Claeys (IMEC), P. Deak (Univ. of Bremen), D. De Salvador (Univ. of Padova), J.M. Hartmann (LETI), M. Horstmann (AMD), M. Hytch (CEMES/CNRS), J. Kittl (Texas Instruments), D. Lenoble (ST Microelectronics), W. Lerch (Mattson Thermal Products), I. Cayrefourcq (SOITEC), A. Nylandsted-Larsen (Univ. of Aarhus), L. Pelaz (Univ. of Valladolid)

Proceedings:
Authors of accepted abstracts will be asked to submit an extended version of their work. The papers accepted after peer reviewing will be published in Materials Science and Engineering B.

Symposium Support:

EU Integrated Project PullNANO (**PULL**ING the limits of **NANO**CMOS electronics)

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PROGRAM VIEW : 2008

MY PROGRAM : 2008

Symposium : I

Front-end junction and contact formation in future Silicon/Germanium based devices

26 May 2008 | 27 May 2008 | 28 May 2008 | 29 May 2008 | 30 May 2008

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09:00	Introduction by the chairperson of the symposia I, J and K: G. Kissinger, F. Cristiano and T. Peaker	
	Joint keynote presentations of the symposia I, J and K : G. Kissinger, F. Cristiano and T. Peaker	
09:15	Silicon Materials Engineering for Advanced Solar Cells Authors : Eicke R. WEBER Fraunhofer Institute for Solar Energy Systems ISE Freiburg, and Faculty for Physics and Mathematics, University of Freiburg, Germany **Resume :** The looming global climate catastrophe due to man-made emissions of CO_2, and increasing prices and limited availability of fossil fuels lead in recent years to a global effort to promote renewable energies in our energy mix. Among the renewable energies, only solar energy is available in sufficient amounts. However, solar energy, especially photovoltaics (PV), is still more expensive than other kinds of renewable and conventional fossil energy. Feed-in tariffs introduced in Germany about 5 years ago have shown to successfully achieve the goal of rapidly increasing PV production volume. However, an unexpected consequence is a shortage of PV modules, mainly due to the limited production capacity of high-purity silicon. In response, the production volume of high-purity silicon is rapidly being ramped up. Part of this additional capacity will be producing so-called solar-grade silicon, using a somewhat simplified process. However, it appears to be possible to take a third route based on upgraded metallurgical, sometimes called 'dirty' silicon. Processing good solar cells out of this kind of material requires to control the higher impurity content, especially of transition metals. Therefore, silicon materials engineering is needed in PV technology not only to improve the conversion efficiency of crystalline silicon solar cells, but also to introduce this promising alternative material into the PV market to ensure sustained rapid growth of the PV market, with fast cost reduction add to my program (close full abstract)	1 1
10:00	Advanced SOI CMOS transistor technology for high performance microprocessors Authors : Manfred Horstmann AMD Saxony LLC & Co. KG, Wilschdorfer Landstraße 101, 01109 Dresden, Germany **Resume :** An overview of state of the art Silicon on Insulator CMOS transistor technology used for 65nm and 45nm volume manufacturing of microprocessors will be given. AMD's unique technology and transistor progression model as well as the key challenges to increase the power efficiency of microprocessor products will be described. For advanced SOI transistors stress engineering has become a standard feature since the 90nm technology node due to gate oxide scaling limitations [1]. Especially techniques which induce local strain such as compressive and tensile stressed over-layer films, embedded-SiGe, and stress memorization, are keys to enhance transistor and product performance. With optimization, the different stressors are highly compatible and additive to each other, improving PMOS and NMOS saturation drive currents by ca. 50% and 30%, respectively [2]. In addition to reducing the lateral and vertical device dimensions advanced (Laser or Flash) annealing has been applied [3]. These anneal processes yield an improved dopant activation for active and gate regions resulting in lower source-drain resistance and gate depletion without any additional diffusion. To achieve a "high performance per watt", technology and design optimization is required. Technology elements like SOI, stressors, multiple gate oxides needed hand-in-hand development with multiple core designs and power efficient microprocessor architectures. These techniques have been applied and optimized for 65nm and 45nm manufacturing and are scaleable to 32nm design rules. Future technology options, like strained silicon directly bonded on SOI, embedded Si:C and High K gate oxide will be discussed. [1] M. Horstmann, et al., IEDM 2005, p. 243 [2] A. Wei et al., VLSI 2007 [3] Th.Feudel et al., RTP Conference, Kyoto, 2006 add to my program (close full abstract)	1 2
10:45	CMOS Scaling into 22 nm and Beyond: Device and Material Requirements and Options Authors : Ghavam G. Shahidi, IBM Research Division **Resume :** CMOS scaling is in the midst of transition that is being imposed by chip operation at cooling limit. The biggest change is moving away from frequency scaling. That is why some people have questioned the viability of Moore\\\\\\\\\\\\\\\'s Law. Despite the power challenge, the density scaling is expected to continue through 15 nm (and beyond) nodes. Performance scaling is also important and that is being traded off for lower power. Non-Si devices have been receiving more attention, because of either higher mobility or higher saturated carrier velocity. The talk is an overview of CMOS scaling trends and challenges, a review of non-Si devices (based on Ge, SiGe, and III-V\\\\\\\\\\\\\\\'s) and some challenges that should be overcome, before they are introduced in high volume. add to my program (close full abstract)	1 3
11:30	NANOSIL Network of Excellence Authors : F. Balestra, IMEP (Grenoble INP, CNRS, UJF)-Sinano Institute Minatec, BP 257, 38016 Grenoble, France **Resume :** The NANOSIL Network of Excellence aims to integrate at the European level the excellent European research laboratories and capabilities in order to strengthen scientific and technological	

excellence in the field of nanoelectronic materials and devices for terascale integrated circuits (ICs) and disseminate the results in a wide scientific and industrial community. NANOSIL explores and assesses the science and technological aspects of nanodevices and operational regimes relevant to n+4 technology node and beyond. It provides a forward-look for the industry, enabling informed decisions to be taken on technology development in order to speed up technological innovation. It encompasses projects on nanoscale CMOS and post-CMOS. The activities are thus centred on the "More Moore" and "Beyond-CMOS" domains but natural links are also established with the other ENIAC areas. Within the Network there are all the critical facilities and expertise to occupy and transcend this space. We propose innovative concepts, technologies and device architectures- with fabrication down to the finest features, and utilising a wide spectrum of advanced deposition and processing capabilities, extensive characterisation and world leading device modelling. This work is 14
carried out through a network of joint processing, characterisation and modelling platforms. NANOSIL's specific objectives are delivery of significant outputs in the following areas: – Appraisal of new channel materials for end of CMOS era – Routes to realisation of Schottky barrier contacts for new source-drain architectures – Identification and appraisal of gate stack materials/combinations for novel gate architectures – Evaluation of the prospects of 1D nanowires for the post-CMOS era – Investigation of the prospects for carbon structures - especially graphene, and their technological potential – Innovative MOS device functionality based on impact ionisation and tunnelling – Investigation of routes for producing high densities of nanodevices by templated self-assembly, and assessment of their technological potential. References: Nanosil European Network of Excellence, FP7, Information and Communication Technologies, Grant agreement no. 216171.

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12:00 Lunch

Devices and Advanced Annealing Schemes : Manfred Horstmann, AMD Saxony

13:45 Issues and challenges for junction optimisation in multi-gate non-planar devices

Authors : T. Hoffmann, IMEC, Kapeldreef, 75, 3100 Leuven, Belgium

Resume : As metal-oxide-semiconductor (MOS) device dimensions scale, control of short channel effects (SCE) and junction leakage become more difficult. When scaling junctions one often trades-off drive versus SCE control and/or leakage. In recent years, millisecond anneals and inventive co-implantation of non-dopant impurities have been employed for successful scaling of ultra-shallow junctions. With each passing technology node the usefulness of the bulk silicon architecture is in question more and more. The ITRS roadmap states that alternative architectures are being considered for future technology nodes. Multi-gate devices such as fin field-effect-transistors (FinFETs) are proving to be a promising approach for scaling MOS devices to sub-30 nm gate lengths. The non-planar architecture can overcome the increased difficulty of controlling SCE at such 21
device dimensions. As the width of this device can be approximated as the sum of the side and the top surface dimensions, optimisation of the side surface (sidewall) doping can add an extra degree of freedom for improved FinFET performance. A conformal deposition and in-diffusion methodology may produce equal doping on top and side surfaces, and techniques such as vapour phase doping or plasma doping could be advantageous in this regard. Ion implantation remains a strong candidate as the means to introduce dopants into the fin, as it is an established and conventional technique. One disadvantage is the angle restriction to avoid shadowing during implant of dense structures. If the ion beam fails to hit the foot of each fin an increase in access resistance will result in a loss of drive current. In this talk the emerging challenges that face junction formation in this 3-dimensional thin-body silicon device architecture will be discussed.

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14:15 ADVANCED ACTIVATION USING VARIOUS THERMAL BUDGET REGIMES SUCH AS FLASH, MULTIPLE FLASHES AND FLASH SPIKE ANNEALING

Authors : W. Lerch, S. Paul, J. Niess, Mattson Thermal Products GmbH, Daimlerstr. 10, D-89160 Dornstadt, Germany S. McCoy, J. Gelpey, Mattson Technology Canada Inc. 605 W. Kent Ave., Vancouver, B.C. V6P6T7 Canada F. Cristiano LAAS/CNRS 7 av. Du Col. Roche, 31077 Toulouse, France P. Pichler, A. Martinez Fraunhofer-IISB, Schottkystrasse 10, 91058 Erlangen, Germany H. Kheyrandish CSMA Ltd, Queens Road, Penkhull, Stoke-on-Trent, Staffordshire ST4 7LQ, United Kingdom D. Bolze IHP, Im Technologiepark 25, 15326 Frankfurt (Oder), Germany

Resume : Millisecond annealing as an equipment technology provides ultra-sharp temperature peaks which favours dopant activation but nearly eliminates dopant diffusion to form extremely shallow, highly electrically-activated junctions. On boron and arsenic beamline-implanted wafers various annealing schemes were investigated for the formation of ultra-shallow and custom-shaped 22
junctions. The main scheme consisted of flash annealing with peak temperatures ranging from 1250 °C to 1300 °C, followed by a spike annealing with peak temperatures in the range from 900 °C to 1000 °C to achieve a desired junction depth. To reduce the sheet resistance of pMOS and nMOS source-drain extensions, combinations of two or three flash anneals in a row were tested. Finally, the standard flash anneal condition of a 750 °C intermediate temperature followed by the flash was changed to a high intermediate temperature of 950 °C followed by the flash anneal up to 1300 °C. The results of all these annealing schemes were analysed by four point probe measurement. Selected samples were analysed by Hall-effect for peak activation, and by secondary ion mass spectrometry for profile shape as well as diffusion effects. Transmission electron microscopy was used to study residual defects. Selected boron and arsenic dopant profiles are also compared to predictive simulation results which address the diffusion and activation at extrinsic concentrations.

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14:45

LASER THERMAL PROCESSING FOR ACTIVATION OF ULTRA SHALLOW JUNCTIONS OBTAINED BY PLASMA IMMERSION ION IMPLANTATION.

Authors : Vanessa VERVISCH1,P.DELAPORTE1, Y.LARMANDE1, T.SARNET1,M.SENTIS1 H. ETIENNE2, F.TORREGROSA2,L.ROUX2 F.CRISTIANO3,P.F.FAZZINI4 1 Laboratoire LP3, UMR 6182, Université de la Méditerranée, Campus de Luminy, Case 917, 13288 Marseille Cedex 9, France. 2 Ion Beam Services, ZI Peynier Rousset, Rue Gaston Imbert prolongée, 13790 Peynier, France 3 LAAS-CNRS, University of Toulouse, 7 av. du Col Roche, 31077 Toulouse, FRANCE 4 CEMES-CNRS, University of Toulouse, 29 rue Jeanne Marvig, 31055 Toulouse, France

Resume : In the past few years, Laser Thermal Processing (LTP) has become an interesting solution in order to activate ultra shallow junctions as required by the International Technology Roadmap for

Semiconductor (ITRS). This paper presents a study combining boron implantation by Plasma Immersion Ion Implantation (PIII) followed by Laser Thermal Annealing. Boron doping was performed by PULSION®, a PIII tool developed by IBS, at low acceleration voltage (1kV) at saturation dose. Then, samples have been annealed by an ArF excimer laser with a wavelength of 193 nm and energy densities varying from 275 to 800 mJ/cm². Secondary Ion Mass Spectrometry (SIMS) and Four-Point Probe (4PP) have been used to determine junction characteristics. After
process (implantation and LTP), boron SIMS profile shows a junction depth of 30 nm and electrical 2
characterizations give a sheet resistance of 593 Ω/sq. To reduce these parameters, Pre- 3
Amorphization Implantations (PAI) by germanium ions have been tested. This allowed a decrease of the junction depth down to 23 nm and a sheet resistance down to 561 ohm/sq. The structural analysis obtained by Transmission Electron Microscopy on sample with and without germanium Pre-Amorphization Implantation (PAI) allowed to determine the thickness of the amorphous layer but also to observe the silicon matrix after LTP. In addition, this paper will present a comparative study with different excimer laser at different wavelegth: ArF (193nm), KrF (248nm) and XeCl (308nm).

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(close full abstract)

15:00 Ultra Shallow Junctions fabrication by Plasma Immersion Implantation on PULSION® followed by Spike and/or Flash Annealing. Effect of pre-amorphization and co-implantation on Boron diffusion in Silicon.

Authors : Hasnaa ETIENNE, Frank TORREGROSA, Guillaume SEMPERE, Gilles MATHIEU, Laurent ROUX- ION BEAM SERVICES, ZI Peynier-Rousset, rue Gaston Imbert Prolongée, 13790 Peynier, France Fuccio CRISTIANO- LAAS-CNRS, University of Toulouse, 7 avenue du Colonel Roche, 31077 Toulouse France Pier-Francesco FAZZINI - CEMES-CNRS, University of Toulouse, 29 rue Jeanne Marvig, 31055 Toulouse France Wilfried LERCH, Silke PAUL - MATTSON Thermal Products GmbH, Daimlerstr. 10, D-89160, Germany Jeff GELPEY, Steve MCCOY-MATTSON Technology Canada Inc. 605 W. Kent Ave., Vancouver, B.C. V6P6T7, Canada Frédéric MILESI, Frédéric GONZATTI- CEA-LETI MINATEC, DRT/DPTS / SDOT, 17 rue des Martyrs 38054 Grenoble cedex 9, France Aron PAP, Krisztián KIS-SZABO, Tibor PAVELKA- SEMILAB Semilab, Inc., 2 Prielle K. str., H-1117 Budapest, Hungary

Resume : Pre-amorphisation and co-implantation have been shown to have a positive effect for the fabrication of highly doped P+/N junctions. On the other hand, interactions between defects and implanted dopants are known to be responsible for the main difficulties to the formation of ultra
shallow junctions (USJs), such as BICs, deactivation, leakage current. This has been already 2
investigated for classical beamline implanted USJs using different annealing processes but not yet for 4
Plasma Immersion Implanted USJs. In this paper we propose to study the effect of amorphization and co-implantation on PULSION® implanted USJs, using different annealing processes in order to remove the damage and get high dopant activation with the lowest diffusion. A classical beamline implanter was used for the amorphization and co-implantation, and PULSION® was used for shallow Boron implantation using BF3 plasma. Then annealing was done by varying the thermal budget using second or millisecond annealing (respectively Spike or Flash RTP). Sheet resistance and junction leakage measurements were done using a non contact electrical characterization tool (SEMILAB). They were complimented by Hall effect measurements to precisely determine dopant activation and carrier mobility. Dopant profiles were studied using SIMS, and TEM was used for defect analysis. This work was done in the frame of the European program PULLNANO, in order to achieve the specifications of 32 and 22 nm technological nodes. The results show that for the same annealing process, PAI reduces sheet resistance while increasing junction leakage with no benefit on junction depth. On the other hand, PAI, added to Carbon co-implantation, induces a decrease in junction depth with an increase of sheet resistance and no effect on junction leakage. One of the best results is obtained with PAI only at the lowest PULSION® acceleration voltage (11nm, 1300 ohm/sq and 3.7x10-8A/cm²).

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15:15 Experimental and simulation study of the flash lamp annealing for boron ultrashallow junction formation and its stability

Authors : K. R. C. Mok#, S. H. Yeong*/#, B. Colombeau#, F. Benistant#,C. H. Poon#, A. See#, C. M. Ng#, L. Chan# and M. P. Srinivasan* 1Chartered Semiconductor Manufacturing Ltd, 60 Woodlands Industrial Park D, Street 2, Singapore 738406 2Department of Chemical and Biomolecular Engineering, National University of Singapore, 9 Engineering Drive 1, Singapore 117576

Resume : Recent works demonstrated that flash lamp annealing (FLA) is able to provide junctions that are highly activated and ultrashallow. However, the thermal budget from the FLA is not enough to fully dissolve the extended defects induced by preamophizing implant. This affects the junction stability upon post-thermal cycle. In this work, the junction stability is investigated through the
de/re-activation behavior of B in the flash annealed junctions subjected to subsequent isochronal 2
annealing. It is shown that a single pulse FLA leads to significant dopant deactivation and it can be 5
reduced by additional of flash pulses or eliminated by prior spike RTA step. To understand the physics underlying the FLA, junction profiles and activation data are examined using kinetic Monte Carlo simulator. The junction stability behaviors from single pulse FLA and prior spike RTA scheme can be well reproduced by the simulation. The distributions of the point defects for various flash conditions were simulated to study and the evolution of defects as well as the physical interactions between defects with dopants during the millisecond flash annealing. For different FLA schemes, the simulated results show distinct variations in extended defect profiles that can be correlated to the different extent of junction stability eventually. In conclusion, a deeper physical understanding has been achieved on the junction formation by FLA through its junction stability study complemented by kMC simulation.

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15:30 Coffee Break

Atomistic Simulations I : Wolfgang Windl, Ohio State University

16:00

Modeling of surface effects on Si amorphization and recrystallization

Authors : Lourdes Pelaz, Luis Marqués, Pedro López, Ivan Santos, María Aboy Universidad de Valladolid, Spain

Resume : The fabrication of low resistive ultra-shallow junctions requires the use of high-dose ultra-low energy implants. As a consequence, damage and dopants are concentrated near the surface, and its influence comes into play. It has been reported that ultra-low energy B implants can cause Si amorphization at room temperature [1]. The amorphous layer grows with dose from the surface rather than from mean projected range (Rp) of the implant. For low-energy heavy-ion (As, Ge) implants, damage accumulates both at the surface and at Rp, producing thicker amorphous layers. In the case of low-energy molecular implants, such as B18H22, damage production is severe near the surface. Even a single cluster impact causes direct amorphization of regions several nm in diameter, the formation of craters at the surface and significant sputtering. Detailed modeling of damage production, accumulation and recrystallization phenomena should be modeled in detail in order to capture these phenomena and develop predictive process simulators. Influence of local melting due to energy deposition on the formation of amorphous regions, the role of the surface on damage accumulation and the dependence of the recombination rate on crystallographic orientation will be analyzed on the basis of kinetic Monte Carlo and Molecular Dynamics simulations. [1] J. A. Van den Berg et al, Nucl. Instrum. Methods Phys. Res. B 183, 154 (2001). 31

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16:30 Modeling by molecular dynamics of the recrystallization of ultrathin silicon amorphous layer and boron diffusion

Authors : C. Krzeminski [1], A. Mattoni [2], E. Lampin [1], F. Cleri [1] and L. Colombo [2] 1 Institute of Electronics, Microelectronics and Nanotechnology (UMR CNRS 8520, and University of Lille I, Villeneuve d'Ascq, 59652 FRANCE 2SLACS-INFM/CNR, Sardinian Laboratory for Computational Materials Science and Department of Physics, University of Cagliari, Monserrato (CA) 09042 ITALY

Resume : Doping implantation into a preamorphized silicon layer followed by solid phase epitaxy regrowth (SPER) or sub-melt laser annealing (LA) are intensively studied for the formation of ultrathin junctions for sub-65 nm technological nodes. The sharp requirements of the ITRS roadmap in terms of resistance, abruptness and depth are expected to be met by an experimental trade-off. Molecular dynamics simulations represent an interesting approach to predict the evolution in such complex processing, and to validate conflicting mechanisms. We report on a joint effort to properly model the recrystallization process by means of atomistic simulations based on model potentials. Firstly, by focusing on the case of a planar a-c interface, we present a comprehensive study of the available model potentials for solid phase epitaxy (SPE) and liquid phase epitaxy (LPE). The analysis takes into account several important physical properties such as the SPE or LPE velocity, the activation energy, the structural properties of the amorphous phase. Examples are discussed in the case of pure silicon and boron doped a-c systems. Next, an atomic scale picture of the incorporation of boron during the recrystallization is also presented. The result shows that boron can be incorporated as substitutional dopant or form clusters with a low content of silicon self-interstitials. A full characterization of the formation process of boron-interstitial clusters and their stoichiometry is presented . 32

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16:45 Atomistic simulation of solid phase epitaxial regrowth in Si: A critical review

Authors : M. Posselt Forschungszentrum Dresden-Rossendorf, Institute of Ion Beam Physics and Materials Research, P.O.Box 510119, D-01314 Dresden, Germany

Resume : During ultra-shallow junction formation, pre-amorphization or dopant implantation may lead to the formation of an amorphous (a-)layer. In the first stage of annealing the solid phase epitaxial regrowth (SPER) of the a-layer takes place. During SPER, redistribution of the dopants occurs, and they are incorporated into crystalline Si (c-Si), either substitutionally or within clusters containing dopant atoms, self-interstitials (Is) and/or vacancies. The SPER process leaves beyond the original a/c interface the end-of-range (EOR) damage which contains an excess of Is. During further annealing, free Is are emitted from the EOR damage and diffuse towards the surface. In this period the diffusion of dopants is considerably enhanced. It is highly desirable to obtain the initial conditions for calculations of dopant diffusion and activation, i.e. the fractions of dopants on substitutional sites and in clusters as well as the cluster morphology, from atomistic simulations of SPER. This work gives a critical review of previous simulations that are based on classical molecular dynamics. It is shown that even for pure Si the experimental regrowth rates cannot be reproduced reasonably well. The main cause for the disagreement is the inaccuracy of the interatomic potentials used. Proposals for physically-based improvements are discussed. They are based on a better description of the amorphous phase using a modified potential, without changing the well-established potential for c-Si. 33

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17:00 Long Hop kinetic Monte Carlo: Techniques to speed up atomistic modeling without losing accuracy.

Authors : Ignacio Martin Bragado. Synopsys Inc. USA Nikolas Zographos. Synopsys LLC. Switzerland

Resume : According to the ITRS, the development of predictive TCAD models and simulators is one of the keystone for future CMOS technologies. The kinetic Monte Carlo (kMC) technique is particularly well placed between the poles of physical ab-initio but very slow simulations, and more empirical, fast simulations by partial differential equations. Nevertheless, in other to fulfill the necessities of the semiconductor industry, kMC simulations have to be faster and more accurate. This work shows techniques to increase the simulation speed of kMC simulations while still maintaining accuracy, reducing the simulation time in average by 60%, and in some cases even by 85%. These techniques modify the original kMC method by using different jump distances and performing several jumps at once during the same simulation cycle. It also shows the problems and limitations of these strategies, how to detect them, and how to overcome them, if possible. Finally, a comprehensive set of simulations - including amorphization, recrystallization, extended defect ripening, diffusion and activation/deactivation of several dopants used in CMOS technologies - with and without speed-up techniques are compared to experimental SIMS to elucidate how reliable these techniques are. 34

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17:15

Defect and dopant kinetics in the laser annealing of Si

Authors : A. La Magna, G. Fisicaro, G. Mannino and V. Privitera Consiglio Nazionale delle Ricerche Istituto per la Microelettronica e i Microsistemi Z.I. VIII Strada 5, I 95121 Catania, Italy B. G. Svensson Department of Physics, Physical Electronics, University of Olso P.O Box 1048 Blindern, N-0316 Oslo, Norway

Resume : Ultra fast thermal processes in Si (from the ms to ns regime), induced by the laser irradiation, attract a widespread interest due to the possibility to complement or substitute the rapid thermal annealing in the activation module of future nanoelectronics devices. However, the post-

implant detailed kinetics of the defects-dopant system in the extremely far from the equilibrium conditions caused by the laser irradiation both in the non-melting and melting regime is almost totally unknown. From the theoretical point of view some relevant questions have to be addresses: the formalization of a reliable kinetic formalism for the evolving defect-impurity system in a non-uniform fast varying thermal field, the generalization of the kinetic parameters (e.g. diffusivity,
clustering rate constants etc) in these conditions, the inclusion in the formalism of the eventual 3
phase transition, the interaction between the defects generated by the implant and the defects 5
generated by the process. In this work a multiscale theoretical approach based of atomistic and continuum descriptions of the problem is applied to investigate these issues. A rigorous derivation of the master equations for the evolution of defect-impurity system is obtained starting from the kinetic Boltzmann’s theory. Early comparison between simulations and mired experiments based on the laser processes are discussed.

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17:30 Stress effects on dopant solubility

Authors : Chihak Ahn/Newcastle University Nick Bennett/Newcastle University Nick Cowern/Newcastle University

Resume : Enhancing dopant solubility is of great interest to ULSI technology and various techniques have been investigated to achieve this goal. Applying a stress is one of the promising techniques and enhanced solubility was reported experimentally. There is still lack of understanding about the exact mechanism. Previously Sadigh et al. claimed using Maxwell-Boltzmann [MB] statistics that B solubility enhancement under biaxial compressive strain is mainly due to a Fermi-level shift [Sadigh
et al. Appl. Phys. Lett. 48, 4728 (2002)]. Near the solid solubility limit, however, even the high 3
temperature effective density of states is comparable to or less than dopant concentrations for 6
shallow dopants and thus MB statistics is not appropriate to describe the system. In this paper, we propose a new explanation for the effect of stress on dopant solubility. Considering the position of the Fermi level near the solubility limit of shallow dopants, we find that the solubility enhancement factor can be determined by only the stress energy that a neutral dopant acquires from the applied strain field due to atomic size mismatch. The enhancement factor of the metastable solubility during solid epitaxial regrowth can also be explained by change in isolated dopant formation energy due to stress. Based on the volume expansion coefficient calculated using density functional theory, the stress dependent solubility enhancement factor is predicted for various dopants and compared with experimental data.

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start at	Subject	Num.
	Characterization : Wilfried Lerch, Mattson Thermal Products	
08:30	New method for quantitative strain mapping at the nanoscale in electronic devices Authors : Martin Hytch, Etienne Snoeck, Florent Houdellier, Florian Hue, Gerard BenAssayag, Alain Claverie CEMES-CNRS, 29 rue Jeanne Marvig, 31055 Toulouse, France **Resume :** Strained silicon is now an integral feature of the latest generation of transistors and electronic devices because of the associated enhancement in carrier mobility. Different ways have been employed to engineer strain in devices leading to complex strain distributions in 2 and 3 dimensions. Developing methods of strain measurement at the nanoscale has therefore been a major goal of recent years but has proven illusive in practice. None of the techniques combine the necessary spatial resolution, precision and field of view. For example, Raman spectroscopy or X-ray diffraction techniques can map strain at the micron scale, and transmission electron microscopy (TEM) at the nanometre scale but over small areas. Here we present a new technique capable of bridging this gap and measuring strain to high precision, with nanometre spatial resolution and for micron fields of view. The method combines the advantages of the conventional moiré technique with the flexibility of off-axis electron holography and is applicable to standard focused-ion beam (FIB) prepared samples. We will present measurements of strain in the active regions of strained-silicon MOSFET devices and compare the results from finite element modelling. **add to my program** **(close full abstract)**	41
09:00	Evidence of the carrier mobility degradation in highly B-doped ultra-shallow junctions by Hall effect measurements Authors : F.Séverac, F.Cristiano, E.Bedel-Pereira, LAAS-CNRS, Université de Toulouse, 7 avenue du Colonel Roche, 31077 Toulouse, France ; W.Lerch, S.Paul, Mattson Thermal Products GmbH, Daimlerstrasse 10, D-89160 Dornstadt, Germany ; H. Kheyrandish, CSMA Manchester, UK. **Resume :** Current fabrication processes of MOS source/drain ultra-shallow junctions (dopant implantation in a preamorphised substrate, followed by ultra-rapid anneals at high temperature) generate defects which can degrade their electrical properties. The understanding of the physical phenomena responsible for this degradation is essential for the optimization of the fabrication processes. Among these phenomena, the impact of Boron Interstitial Clusters (BICs) on the carrier mobility has not yet been clearly understood. In this work, we present an empirical method for the self-consistent interpretation of SIMS and Hall effect measurements of boron doped ultra-shallow junctions that allows to estimate the activation level of the doped layers (maximum active dopant concentration, active dose fraction) and, for the case of partially activated structures, to assess whether or not the carrier mobility is affected by the electrically inactive BICs. Both epitaxial and implanted structures were studied. We found that, depending on the fabrication conditions, the maximum active dopant concentrations extracted from the studied samples may differ from the boron solid solubility at the process temperature. In addition, for the partially electrically active structures, a degradation of the drift mobility due to the presence of BICs is shown, which is experimentally confirmed by low temperature Hall effect measurements, indicating the existence of an additional Coulomb-type scattering mechanism. **add to my program** **(close full abstract)**	42
09:15	Differential Hall Characterisation of Ultrashallow Doping in Advanced Si-Based Materials Authors : N. S. Bennett, N. E. B. Cowern (School of Electrical, Electronic and Computer Engineering, University of Newcastle, Newcastle upon Tyne, NE1 7RU, UK). M. Kah, A. J. Smith, R. M. Gwilliam, C. Jeynes, R. P. Webb, B. J. Sealy (Ion Beam Centre, University of Surrey, Guildford, GU2 7XH, UK). T. C. Q. Noakes, P. Bailey (Daresbury Medium-Energy Ion Scattering Facility, Daresbury Laboratory, Warrington, WA4 4AD, UK). D. Giubertoni, M. Bersani (Fondazione Bruno Kessler, Via Sommarive 18, 38050 Povo-Trento, Italy). **Resume :** Strained-Si channels are commonly used by manufacturers to enhance CMOS performance and research into novel channel materials (SiGe & Ge) is well underway. How these materials affect the behaviour of the impurities used to dope them is largely unclear and the ability to accurately characterise dopant activation is key to finding this out. In the case of Si, since much is known about the relationship between carrier concentration and mobility, dopant activation can be assessed by techniques such as spreading-resistance profiling. However for the newer materials this information is not available. Our study demonstrates that the differential Hall technique can satisfy these gaps in our knowledge of dopant activation and mobility. Previously we have shown the technique, which combines Hall-effect measurements with successive native-oxide removal, can measure independent carrier and mobility profiles with resolution <1nm for B-implanted Si and SOI. Presently we show the technique is extendable to characterise n-type dopants (As & Sb) and importantly, can be applied to novel substrates (strained-Si, SiGe & Ge). In addition, the inherent assumption of the technique - uniform layer removal - is investigated and shown reasonable. Complementary ion beam analysis is used to show how we can correct for Hall scattering effects. Designated software is used to correct for carrier surface-depletion, transforming raw data into reproducible and highly resolved, carrier and mobility profiles.	43

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09:30 2D-CARRIER PROFILING WITH SUB-NANOMETER RESOLUTION IN ADVANCED DEVICES USING HIGH VACUUM SCANNING SPREADING RESISTANCE MICROSCOPY

Authors : Pierre Eyben(a), Jay Mody(a,b), Danielle Vanhaeren(a) and Wilfried Vandervorst(a,b) (a) IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (b) KU Leuven, Electrical Engineering Dept., INSYS, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

Resume : Scanning spreading resistance microscopy is a two-dimensional carrier profiling technique now widely used for the characterization of semiconductor materials and in particular of silicon devices. SSRM offered already a unique combination of resolution (spatial resolution of 1–3 nm and a dopant gradient resolution of 1-2nm/dec), and of sensitivity (around 20%) over a wide
dynamic range (10E15 to 10E21 at/cm3). Recently a High Vacuum-SSRM (HV-SSRM) version has 4
been developed with further improved performance relative to the ambient version. Use of vacuum 4
(10-5 torr) reduces the presence of contaminants on the surface of the sample, avoids the deposition of a water layer due to the natural humidity of air and thus avoids the growth of native oxide. Not only the quality of the electrical contact and the signal/noise ratio is improved but also the spatial resolution as lower forces can be used limiting the sample and tip damage. Thus, using the advantages of the HV-SSRM we have demonstrated for the first time two-dimensional carrier profiling with sub-nanometer spatial resolution. Using the advanced HV-SSRM we have studied the doping/carrier profile engineering for sub-45nm MOS devices using various doping (implantation, cocktail implants, PAI, plasma doping) and annealing technologies (spike, laser anneal,..).

add to my program **(close full abstract)**

09:45 Three-Dimensional Atomic scale imaging of boron clustering in crystalline silicon

Authors : M. Ngamo(1), O. Miredin(1), E. Cadel(1), S. Duguay(1), R. Lardé(1), K. Daoud-Ketata(1), P. Pareige(1), D. Blavette(1), F. Cristiano(2), D. Mangelinck(3). 1: Groupe de physique de matériaux, Université et INSA de Rouen, UMR 6634, Avenue de l'université, 76801 saint Etienne du Rouvray, France. 2: Laboratoire d'analyse et d'architecture des systèmes du CNRS, 7 avenue du colonel roche, 31077 Toulouse Cedex 4, France. 3: Institut Matériaux Microélectronique Nanoscience de Provence, Université Aix-marseille, UMR 6242, Avenue Escadrille Normandie Niemen - Case 142, F - 13397 Marseille Cedex 20

Resume : The fabrication of p-type ultra-shallow junctions in recent MOS technologies requires the use of high boron (B) implantation fluencies and low thermal budget. In those conditions, B-
clustering is a well-known phenomenon that limits its diffusion and activation. These boron 4
interstitial clusters (BIC) are too small to be visualized even with high-resolution transmission 5
electron microscopes. Today, the Laser Assisted Wide-Angle Tomographic Atom Probe (LAWATAP), developed in our laboratory, is a unique technique that allows the observation and chemical analysis of these BIC's with atomic resolution. A description of the basic principles of the technique will be first presented, including specific sample preparation issues. Then, optimised experimental conditions were defined on the bases of simulation to create a sufficiently high density of BIC's in Si. The first results obtained on B-implanted silicon show a non-homogeneous distribution of B with a tendency to clustering. The obtained results will be correlated to those given by SIMS in order to take advantage of the accuracy of the 3D-LAWATAP analysis for a better understanding of boron activation anomalies.

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10:00 Coffee Break

Silicides and Germanides : Anne Lauwers, IMEC

10:30 Silicides and Germanides for Nano-CMOS Applications

Authors : J. A. Kittl, K. Opsomer, C. Torregiani, C. Demeurisse, S. Mertens, C. Vrancken, M. J. H. van Dal* and A. Lauwers IMEC, *NXP

Resume : Silicides have been used in Si-based CMOS devices for many generations, as contacting materials for source, drain and gate electrodes. Ti and Co led way to Ni-silicides due to scaling limitations of C54 TiSi2 and CoSi2, mainly the inability to form the target silicide phase in small gates. NiSi was for this reason introduced for devices with sub-40 nm gate lengths. Issues with the implementation of Ni silicide, such as thermal stability and encroachment will be presented, showing the advantages of moving to Ni-alloy silicides such as (Ni-Pt)Si or of the addition of impurities such as C. With the introduction of SiGe in source-drain areas, the interest in
germanosilicides increased, finding here as well advantages of Ni-alloys over Co-based materials, 5
but finding, however, a reduction in the process window with the addition of Ge. With the 1
introduction of metal gates, requirements change. The need for low gate sheet resistance is no longer a constraint, and optimization of the silicide or germanosilicide is only evaluated in terms of its performance as source and drain contacting material. The need for further reduction of parasitics, specifically silicide to source/drain contact resistivity, motivated research on low Schottky barrier alternatives such as rare earth or noble metal silicides, as well as the incorporation of these materials in Ni-based silicides. Studies on substrates with high concentrations of activated dopants, did not show, however, the anticipated advantage of these materials. Recently, the increase in interest in Ge devices, motivated by their high mobilities, lead to increased activity in the study of germanides. In this paper, an overview of these topics will be presented.

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11:00 Self Aligned Nickel-Platinum Silicide Oxidation

Authors : B. Imbert1,2,3, S. Zoll3, P. Garnier3, B. Pernet3, D. Galpin3, R. Beneyton3, M. Juhel3, P. Mur4, V. Carron4, O. Thomas1,2 1Aix-Marseille Université, IM2NP 2CNRS, IM2NP (UMR 6242), Faculté des Sciences et Techniques, Campus de St Jérome, F-13397 Marseille Cedex, France 3STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles cedex, France 4 CEA-LETI, MINATEC, 17
rue des Martyrs, 38054 Grenoble Cedex 9, France 5

Resume : Nickel silicide is now widely used in advanced devices thanks to its low temperature 2
formation, low resistivity and silicon consumption. After Ni(Pt) (5% at.) deposition, silicidation is obtained during an anneal step followed by selective wet etch to remove un-reacted Ni(Pt). For specific process conditions, a silicon oxide layer is observed at the end of the process instead of the expected nickel silicide. The aim of this study is to analyse the transformation mechanism resulting from the interaction between selective etch chemistry and Ni(Pt) silicide. During Hydrochloric Peroxide Mixture (HPM) dispense the silicide layer is transformed into a rough oxide film. TEM cross

section evidences a silicide-oxide bilayer stack on polySi gate resulting in a line resistance increase modulated by anneal temperature and features dimensions. The proposed mechanism for this oxide formation is a galvanic corrosion in HPM in presence of Ni rich silicide and Pt. Ni and Si form the anode and Pt the cathode. Ni and Si are both oxidized whereby Ni is dissolved while Si oxides are insoluble and remain on the surface.Pt accumulates at the surface of Ni-rich silicide phases for temperature below NiSi phase transition. At higher anneal temperature Pt is incorporated in NiSi. This Pt migration could explain why there is no silicide oxidation when the NiSi is formed. HPM conditions are presently being investigated to find a compromise between Pt strip efficiency and inhibition of oxide formation.

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(close full abstract)

11:15 Impact of channel doping on Schottky barrier height and investigation on p-SBMOSFETs performance.

Authors : G. Larrieu (1), E. Dubois(1), D. Yarekha(1), N. Breil(1), N. Reckinger(2), X. Tang(2), J. Ratajczak(3) and A. Laszcz(3) (1) IEMN, UMR CNRS 8520, Avenue Poincaré, Cité Scientifique, 59652 Villeneuve d'Ascq Cedex, France (2) UCL, Place du Levant, 3, Maxwell Building, B-1348 Louvain-la-Neuve, Belgium. (3) Institute of Electron Technology, Al. Lotników 32/46, 02-668, Warsaw, Poland.

Resume : Metallic Source/drain MOSFETs have aroused a renewed interest due to its capabilities to solve challenges associated to S/D CMOS scaling, owing to its interesting properties (low Rcontact, low Rsheet and infinite abruptness) and drastic process simplification (no S/D implantation). To be
competitive, the Schottky barrier height (SBH) should be below 0.1 eV but currently, using PtSi or 5
$ErSi_{2-x}$, the SBH saturates at 0.15 eV, in the best case. This paper proposes to study the impact of 3
a moderate variation of the channel doping level on electrical performance. First, it has been found that a moderate increase of the doping level leads to a reduction of the SBH but do not affect the silicide reaction. In the case of PtSi, the SBH on p-type silicon at $5\ 10^{15}$ cm-3 is 0.15 eV whereas an increase of two decades of the doping level decreases the barrier by 50 meV. The integration of PtSi MOSFETs on moderately doped channel ($5\ 10^{17}$ cm-3) was successfully achieved, demonstrating an overall 50% improvement in current drive at Lg=110nm. This enhanced performance is attributed to the barrier height reduction related to the beneficial band bending induced by p-type dopants. These doping levels are still in the low range to not affect the carrier mobility in the channel. A complete study, including comparison of Ion, Ioff, immunity against short channel effects (Swing and DIBL), is presented.

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(close full abstract)

11:30 Nickel silicides and germanides: Phases formation, and kinetics and thermal expansion

Authors : C. Perrin*, D. Mangelinck*, F. Nemouchi*, J. Labar**, C. Lavoie***, C. Bergman*, P. Gas* * Institut Matériaux, Microélectronique et Nanosciences de Provence, IM2NP-UMR CNRS 6242, case 142, Faculté de saint Jérôme, 13397 Marseille cedex 20, France ** Research Institute for Technical Physics and Materials Science (MFA) H-1121, Budapest, Konkoly-Thege M. út 29-33, Hungary *** IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598, USA

Resume : Thin film germanide reactions are often declared to be the same as silicides reactions which were far more studied. It is usually reported that the growth of thin film nickel germanides is sequential with two phases in the sequence: the first one is a Ni-rich phase, then the monogermanide NiGe grows. In this paper, we present a comparative study of the phase formation and kinetics of nickel silicides and nickel germanides by several experimental techniques. The samples, composed of a nanometric nickel film (10-50 nm) deposited on silicon or germanium
substrates, have been examined by several "in situ" real time measurements: X-ray diffraction 5
(XRD), four point probes resistance and differential scanning calorimetry (DSC). They have been 4
also characterized by "ex situ" XRD and TEM. Original DSC and "in situ" XRD measurements have allowed us to determine the interfacial reaction rate for Ni_2Si using a linear-parabolic law. During the relatively fast DSC ramp, the growth is mainly controlled by the interface while isothermal heat treatments lead to a mainly diffusion control. In contrary to what is usually found for nickel silicide and germanides, a simultaneous growth of Ni_5Ge_3 and NiGe has been found during "in situ" XRD measurement. The different behavior between the Ni-Si system (sequential formation) and the Ni-Ge system (simultaneous formation) will be interpreted in term of diffusion and interface controlled growth. In addition, an important physical characteristic of NiSi is the anisotropy of dilatation coefficient with a negative component along the b axis. This can affect the film stability and the stress in devices. In this work, the lattice parameters and linear thermal expansion coefficients of the orthorhombic $Ni(Si_{1-X}Ge_X)$ compounds with $0 \leq x \leq 1$ were determined from high temperature X-ray diffraction data (298 K-1073 K). A negative thermal expansion coefficient of the b lattice parameter of $Ni(Si_{1-X}Ge_X)$ for all the studied Ge concentration was observed: the magnitude of this negative thermal expansion coefficient is decreasing with increasing Ge concentration.

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(close full abstract)

11:45 Investigation of NiGe Formation and Defects on Patterned Germanium Device Wafers

Authors : David P Brunco, Brice De Jaeger, Gillis Winderickx, Marc Meuris. IMEC, B-3001, Leuven, Belgium

Resume : Germanium offers better bulk electron and hole mobilities than Si and is a potential replacement for Si in future high performance MOSFETs. In order to realize this potential, low resistance contacts to the source and drain are necessary to minimize series resistances. In this work, we investigate NiGe formation on patterned device wafers using substrates of 2 micron thick epi Ge on Si. The presence of topography in device wafers gives rise to defect modes that are not
observed in blanket test wafer experiments. In particular, we find that annealing 10 nm Ni on 5
patterned SiO_2 structures at more than ~300°C for 30 s gives rise to undesired germanide 5
formation over the patterned SiO_2 and massive voiding in the Ge next to the SiO_2. These results are explained in terms of a Ge diffusion model. We show that a revised process flow involving a low temperature anneal, a selective etch of unreacted Ni, and a higher temperature anneal eliminates this defect mode. Another defect mode involves the formation of voids in the germanium next to the SiO_2 isolation and under the spacers. These voids are not associated with any germanide overgrowth and are more difficult to control. They can be 50 nm deep under the spacers and can therefore seriously degrade performance of short channel devices. In this paper we discuss the role of thermal budget, spacer conditions, and Ni thickness on these voids.

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12:00 Schottky-barrier height tuning of NiGe/n-Ge contacts using As and P segregation
Authors : M. Mueller, Q. T. Zhao, C. Urban, C. Sandow, S. Lenk and S. Mantl Institute of Bio- und Nanosystems and CNI – Center of Nanoelectronic Systems for Information Technology, Forschungszentrum Jülich GmbH, D-52425 Jülich, Germany
Resume : Germanium is a viable solution as future channel material due to its high carrier mobility, the availability of high-k dielectrics and the compatibility with Si technology. In this regard, we investigated doped NiGe/n-Ge(100) contacts which are needed for Schottky barrier MOSFETs. Here we present a systematic study of the Schottky barrier lowering induced by dopant segregation during nickel germanidation. Diodes were fabricated on n-Ge(100) substrate. We used two different
doping ions: As and P (at energies of 10 and 5keV respectivly and various doses) and two different 5
Ni layer thicknesses: 15nm and 30nm. The annealing was done at 400°C for 45s. The formation of 6
the NiGe phase was confirmed by XRD, RBS and TEM measurements. NiGe exhibits a smooth interface to the Ge substrate and a very low specific resistance of 15.1μΩcm, a value similar to NiSi layers formed on Si substrates. The successful segregation was observed by an increase of the reverse currents in the I-V curves. The current of the 30nm NiGe was slightly higher but comparable to the current of the 60nm NiGe layer indicating an independence of the layer thickness. The doping segregation process of both ions species was confirmed by SIMS. Interestingly, the Schottky barrier lowering effect is stronger for As than for P. From low-temperature measurements, significant effective Schottky-barrier height lowering from 0.72eV to 0.19eV for As and to 0.36eV for P was extracted.

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12:15 Lunch

Engineering Substrates : Thomas Hoffmann, IMEC

13:45 Engineered substrates for CMOS applications.
Authors : Dr Ian Cayrefourcq, SOITEC; Dr Nicolas Daval, SOITEC; Dr Laurent Clavelier CEA-LETI; Dr Olivier Faynot, CEA-Leti
Resume : Regardless if Moore's law is coming to an end or not, it is a fact that disruptive innovations, in various fields such as design, device processing or material engineering, need to complement classical scaling to sustain the performance enhancement roadmap of the semiconductor industry. In this paper, we will focus on the role of engineered substrates in this quest for performance. We will first review the well known strain engineering technique. We will
present data from both fully depleted and partially depleted devices obtained both on sSOI 6
(1.3GPa) and XsSOI (1.8 GPa) showing incremental gain. We will show data on the implementation 1
of process induced stressor on sSOI demonstrating that these two techniques are additive. Then , we will go one step further down the roadmap looking at channel material engineering. After reviewing the high potential of such solutions consisting in selecting the best channel material for each device type, we will focus on one example based on Ge alloy channel for PMOS. We will present and discuss both process integration challenges and device data demonstrating how starting from a sSOI template one can obtain high performance PMOS. Finally, we will finally conclude by discussing the main challenges to integrate pure Ge MOSFET and give some outlook through preliminary Ge MOSFET data.

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14:15 Observation of more mobile and conductive holes in strained Ge epilayers than electrons in strained Si ones at room-temperature
Authors : M. Myronov, K. Sawano and Y. Shiraki Research Center for Silicon Nano-Science, Advanced Research Laboratories, Musashi Institute of Technology, 8-15-1 Todoroki, Setagaya-ku, Tokyo 158-0082, Japan
Resume : Over the last years the modulation doped (MOD) heterostructures with a strained Ge quantum well (QW) grown on underlying Si(001) substrate via implementation of intermediate relaxed SiGe buffer have been exhibiting significant progress in enhancement of low- and room-temperatures two-dimensional hole gas (2DHG) mobilities. For achieving high performances at
room-temperature in dramatically scaled down Si-based Field Effect Transistor (FET) devices, 6
however, not only higher carrier mobility but also higher carrier density are required in order to 2
increase carrier conductivity. In this work, we obtained an extremely high room-temperature two-dimensional hole gas (2DHG) drift mobility of 3100 cm2V-1s-1 with very high density of 4.1e12 cm-2 in a MOD compressively strained Ge QW and high two-dimensional electron gas (2DEG) drift mobility of 2900 cm2V−1s−1 with density of 1e11 cm-2 in a MOD tensilely strained Si QW. The p-type Ge QW and n-type Si QW MOD SiGe heterostructures were grown on Si(001) substrates by MBE. Obtained 2DHG mobility is higher and the carrier density is about 8 times larger than those reported before. It is noted that higher carrier density resulted in the breakthrough enhancement of 2DHG sheet conductivity up to 2.04 mS. It is also noted that obtained values are not only the highest ones among 2DHG in a strained Ge QW but also larger than those of 2DEG in a strained Si QW. Obtained extremely high room-temperature 2DHG mobility exceeds three-dimens

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14:30 Structure and electrical properties of strained Si overlayers prepared via lattice mismatched oxide heterostructures on Si
Authors : O. Seifarth*, B. Dietrich*, A. Giussani*, G. Weidner*, P. Zaumseil*, P. Storck\', H.-J. Müssig*, and T. Schroeder* * IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany \'Siltronic AG, Hanns-Seidel-Platz 4, 81737 München, Germany
Resume : Strained Si is an important approach to extend the usability of Si based microelectronics
into new innovative areas. Alternatively to the common SiGe approach to create strained Si layers, 6
we developed a sophisticated (Pr2O3)1-x(Y2O3)x (x = 0 to 1) buffer oxide heterostructure, which 3
allows a flexible tuning of the lattice constant by ± 2.4% around the Si value. Here, we present a fundamental physics study on compressively strained epi-Si(111) layers, created by epitaxial overgrowth on lattice mismatched Y2O3 / Pr2O3 / Si(111) heterostructures, to evaluate the feasibility of our approach. With XRD we prove the single crystalline nature of the atomically smooth epi-Si(111) films, exhibiting a sharp (7x7) surface reconstruction. Raman spectroscopy in combination with Grazing Incidence XRD was applied to monitor in an epi-Si(111) film thickness dependent study the interplay of the strain in the epi-Si(111) film with respect to the lattice

mismatched oxide heterostructure. In case of thin epi-Si(111) films (< 200 nm), strained epi-Si (111) films with a compression of up to 0.4 GPa can be prepared on the oxide heterostructure. In case of thicker epi-Si(111) films (> 200 nm), the lattice mismatch stress is widely adsorbed in the oxide heterostructure and the epi-Si(111) layer grows in consequence fully relaxed. Hall measurements were applied to correlate these structure insights with the electrical properties of the single crystalline epi-Si(111) films of various thicknesses.

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14:45 Session Break

Advanced Layer Growth : Arne Nylandsted Larsen, Aarhus University

15:00 Reduced Pressure – Chemical Vapour deposition of Si / SiGe heterostructures for microelectronics purposes

Authors : J.M. Hartmann et al. CEA-LETI, MINATEC, 17 Rue des Martyrs, 38054 Grenoble Cedex 9, France

Resume : In this invited talk, I will describe some of the epitaxial processes we have developed the last 6 years or so in CEA-LETI for advanced wafers and devices. After a general introduction, I will present some features of SiGe chemical vapour deposition and show how SiGe channels can boost hole mobility by 2 in p-MOSFETs. I will then detail the selective epitaxial growth process we use to form Si or Si0.7Ge0.3:B recessed or raised sources and drains on ultra-thin patterned SOI. I will
also present the specifics of the SiGe virtual substrates and of the tensily-strained Si layers grown 7
on top used as templates for the elaboration of tensily strained-SOI wafers (by SOITEC). The tensile 1
strain, which can be tailored from 1.3 up to 3 GPa, leads to an electron mobility gain by a factor of 2 in n-MOSFETs built on top. High Ge content SiGe virtual substrates can also be used for the elaboration of compressively strained Ge channels, with (when capped with Si) impressive hole mobility gains (x9) compared to bulk Si. After that, I will describe the main features of thick Ge layers grown directly on Si that can be used as donor wafers for the elaboration of GeOI wafers or as the active medium of near infrared photo-detectors. Finally, I will show how Si/SiGe multilayers can be used for the formation of 3D devices such as multi-bridge channel FETs, the SiGe sacrificial layers being removed thanks to plasma etching or by the in-situ gaseous HCl etch method we have recently developed.

add to my program **(close full abstract)**

15:30 Unconventional MODFET structure method of achieving thin Si1-xGex relaxed layer with abrupt N-type doping

Authors : I. Berbezier, J.P. Ayoub, A. Ronda Université Aix Marseille, CNRS, IM2NP UMR 6242, Campus de Saint Jérôme, Avenue Escadrille Normandie Niemen - Case 142, 13397 Marseille Cedex 20, Fr M. Oehme, K. Lyutovich, E. Kasper Institut für Halbleitertechnik, Pfaffenwaldring 47, 70569 Stuttgart, De M. Di Marino, M. Berti Dipartimento di Fisica dell\'Università di Padova via Marzolo 8 35131 PADOVA - It

Resume : We implement a low temperature growth technique for achieving abrupt n-type doping profiles in order to match the proper vertical scaling of the modulation doped field effect transistor fully depleted structure required for ultra-high speed performances. We use strain engineering of
Ge rich Si1-xGex layers to fully incorporate N-type dopant (antimony) at low temperature by 7
suppression of surface segregation. We show that at temperatures below the transition between 2
equilibrium and kinetically limited segregation, in the terrace-mediated kinetically limited segregation regime (T ~ 200°C) ultra-thin highly doped layers can be achieved when they are fully relaxed or biaxially tensily stressed. Such a result is not observed at higher temperature in the step-edge mediated kinetically limited regime where the exchange rate at step edge is almost independent of biaxial stress state. At even higher temperatures used in conventional chemical vapour deposition (350°C and more), N-type dopants surface segregation follows the classical equilibrium law where segregation is mainly controlled by the reduction of surface energy and does not depend on stress. At such temperatures the high segregation coefficient induces dopant profile broadening.

add to my program **(close full abstract)**

15:45 Investigation of the relaxation behavior of Si1-xCx alloys during epitaxial UHV-CVD growth

Authors : Ina Ostermay (a), Thorsten Kammler (b) (a)Fraunhofer Center Nanoelectronic Technologies, Königsbrücker Str. 180, D-01099 Dresden (b) AMD Saxony LLC & Co. KG, Wilschdorfer Landstraße 101, D-01109 Dresden

Resume : Silicon-Carbon is being widely investigated as source/drain stressor to enhance NMOS performance. Since the solid solubility limit is very low, it is challenging to create layers in the required range of substitutional Carbon. In this work, the epitaxial deposition of Si1-xCx alloys by an Ultra High Vacuum Chemical Vapor Deposition (UHV-CVD) system was studied. The carbon fraction in the Si1-xCx layers was controlled by the flux of Methylsilane. Si1-xCx layers with up to
4,6% total Carbon were grown in a temperature range of 550-650°C and characterized using SIMS, 7
rocking curve x-ray diffraction (XRD) as well as Fourier transform infrared spectroscopy (FT-IR). It 3
was found that with increasing the Methylsilane flow the amount of substitutional Carbon passes a maximum at a certain critical value independent of temperature and process pressure. By FTIR, the excess Carbon was determined not predominantly to reside on interstitial sites but to form 3C-SiC precipitates in-situ. A strong relation between the increase of Methylsilane flow and the formation of coherent precipitates even at low carbon fractions was found. Furthermore, the loss of the crystalline integrity due to the generation of carbidic precipitates was observed as the Methylsilane flow exceeds a certain limit. By TEM, these 3C-SiC precipitates were found to degrade the strained layers by forming partially polycrystalline distorted regions. The deposition temperature was found not to influence the amount of coherent 3C-SiC precipitates which is in contradiction to the majority of publications.

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16:00 Coffee Break

Poster Session : Thomas Feudel, AMD Saxony

16:30 Ultra Shallow junctions formation by Boron and Germanium co-implanted in polysilicon on silicon during R.T.A.

Authors : A. Merabet (1), and J. Marcon (2) (1)Laboratoire de Physique et Mécanique des Matériaux

Métalliques, Département d'O.M.P., Faculté des Sciences de l'Ingénieur, Université de Sétif, (19000)
Sétif, Algérie. (2) Laboratoire Electronique Microtechnologie et Instrumentation (LEMI), Université
de Rouen, 76821 Mont Saint Aignan, France.
Resume : The formation of thin junctions is realised by germanium (10E16 atoms/cm2; 100 Kev)
and boron (10E16 atoms/cm2; 25 Kev) co-implanted in 380 nm ploysilicon laid by LPCVD. After
that, we carry out a rapid thermal annealing for 1-20 s at temperatures ranging from 1000 to
1150°C. Preamorphisation with germanium prior to the boron implant has several advantages for
the fabrication of ultra-shallow junctions, suppressing channelling and leading to a high activation of
dopants with low temperature anneals and minimal diffusion. The thermal treatment has been
performed in a 30 KW ADDAX R1000 machine under Argon atmosphere. The samples are then 8
analysed by secondary ion mass spectroscopy (SIMS) CAMECA IMS-4f of Lyon-France. During my 1
preceding works, I have observed the slow down of the boron diffusion with arsenic presence. This
delay becomes more important when the latter dose increases. This study was carried out in the
aim to test the possible electrical interactions between the boron and the arsenic during annealing.
We have implanted the germanium instead of the arsenic. This choice is based upon the electrical
neutrality of this dopant in the silicon. The boron with the presence of the germanium has reached
the same diffusion depths as seen in the case of the boron-arsenic co-implanted in spite of using
the germanium dose five times superior than the arsenic one. This result justifies the using of the
germanium in order to obtain ultra-shallow junctions and highly doped.

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(close full abstract)

16:30 SPECTROSCOPY OF METAL RELATED LEVELS IN Ge BY TRANSIENT INFRARED AND MICROWAVE
ABSORPTION TECHNIQUES

Authors : E. Gaubas1*), A. Uleckas1), and J. Vanhellemont2) 1) Vilnius university, Institute of
Materials Science and Applied Research, Lithuania 2) Department of Solid State Sciences, Ghent
University, Krijgslaan 281 S1, B-9000 Ghent, Belgium *) corresponding author e-mail:
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Resume : Transition metals are fast diffusing contaminants in germanium and may cause
inhomogeneties of recombination parameters within device structures. This can lead to U-shaped
depth profiles throughout the wafer thickness. These metal impurities can be the source of several
deep and shallow recombination centers in Ge. In view of the recent interest to use Ge in advanced
CMOS devices, there is a revival of the investigation of metal related recombination centers. The
aim of the present work is a spectral analysis of recombination centers in n-Ge implanted Co, Fe, Ti, 8
Ni, and Cr by using different implantation doses and post-implantation anneals. The impact of the 2
metallic impurities on the carrier lifetime is studied by combining the measurements of microwave
transients and infrared absorption. Carrier decay transients have been examined by applying
different excitation and bias illumination regimes and were measured both by depth-integrated and
cross-sectional scan modes. It is shown that high densities of implantation related defects can be a
reason for the redistribution of carrier capture and recombination flows by trap filling and charge
sign inversion effects when recombination processes are more complicated than the Shockley-Read-
Hall mechanism. It is shown that the electrical activity of the metal induced recombination defects
depends strongly on the thermal processing of the material after metal implantation. Spectral and
exposure characteristics of photoconductivity quenching have been examined to separate the
competing carrier capture centers induced by the implanted metals.

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(close full abstract)

16:30 The effect of germanium doping on the evolution of defects in silicon

Authors : C.A. Londos1, A. Andrianakis1, V. Emtsev2 , H. Ohyama3 1 University of Athens, Solid
State Physics Section, Panepistimiopolis Zografos, Athens 157 84, Greece 2 Ioffe Physicotechnical
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Russia 3 Kumamoto National College of Technology, 26592, Nishigoshi, Kumamoto 861-1102,
Japan
Resume : Nowadays, silicon is the most important material in electronic industry. It is employed in
a wide variety of applications. However, modern electronics and microelectronics face problems with
corresponding Si-based devices especially concerning high speed operation, low noise level, high
operating frequencies, as well as the increased demand for higher radiation hardness and thermal
resistance. All these problems, coupled with the need of low manufacturing costs, pose the
necessity of creating new materials. In this context, doping of silicon with isovalent impurities
attract considerable interest. These impurities are electrically inactive and they do not exert strong
influence on initial parameters of materials. However, the elastic strains introduced in materials due
to their different atomic size than that of regular atoms can effectively change interactions of
impurities with intrinsic defects such as vacancies and self-interstitials. This property of isovalent
impurities can be used to affect and somehow control interactions between point defects during
crystal growth as well as under irradiation and annealing. Oxygen is the most important impurity in
commercial Czochralski grown silicon. It is electically inactive. However, during irradiation or/and 8
heat treatment various oxygen-related defects, especially multioxygen-multivacancy complexes 3
VnOm, are formed. The majority of these defects are electrically active, exerting strong effects on
electrical properties of Si materials. On the other hand, it is known that the introduction of Ge into
silicon gives rise to compressive strains in the lattice, since the isovalent Ge atoms are larger in
atomic size. As a result, they are effective traps for vacancies. Therefore, the formation and
annealing of VnOm defects is expected to be influenced by the Ge presence.The aim of this work is
to investigate these effects. To this goal, Ge-doped Si samples with various Ge concentrations in
the range 1?017 to 2?020 cm-3 were used. They were irradiated with 2 MeV electrons at a dose of
5?017 e-/cm2. The irradiation temperature was 95oC. After the irradiation, the samples were
subjected to isochronal annealing up to 650oC, in steps of □T= 10oC and □t= 20 min. After each
annealing step, IR absorption spectra were recorded by means of a FTIR spectrometer. As a result
of irradiation, vacancy-oxygen (VO) pairs are formed. Their presence in the spectra is verified by
the 830 cm-1 IR band. Upon annealing this band begins to decay and another band at 888 cm-1,
attributed to the VO2 defect, begins to grow in. The relevant reaction is . It has been established
that the temperature of the VO2 defect formation is markedly reduced due to the presence of Ge
atoms. Whereas this reduction is relatively small for [Ge] up to ~4x1018 cm-3, it is clearly
pronounced for higher [Ge]. On the other hand, the annealing temperature of VO defects, especially
in materials with high [Ge] contents, was found to be even lower than the corresponding
temperature of the VO2 defect formation, indicating that another defect reaction is also running in

the annealing processes of VO complexes: . This phenomena could be reasonably explained if one takes into account an influence of elastic strains due to Ge atoms in the Si lattice on the rates of both principal reactions, i.e. VO Oi → VO2 and VO SiI → Oi . They govern the resultant annealing rate of VO defects, since the migration energy of VO defects in the first reaction and the binding energy of self-interstitials at large agglomerates in the second reaction are believed to be sensitive to the Ge concentration in Si.

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(close full abstract)

16:30

Low frequency noise spectroscopy of interfacial defects in advanced Si and Si/SiGe(C) bipolar transistors

Authors : J. Raoult*, F. Pascal*, M. Marin** *IES, CNRS-Université UMR5214, Place E. Bataillon, 34095 Montpellier cedex 5, France jeremy.raoult@ies.univ-montp2.fr; phone 33(0)467143820 **STMicroelectronics 850 rue Jean Monnet, 38926 Crolles cedex, France

Resume : The aim of this paper is to present the Low Frequency Noise (LF noise) measurement technique as a tool to investigate defects in advanced Si /SiGe Heterojunction Bipolar Transistors (HBTs) and advanced Si Homojonction Bipolar Transistors (BJTs). Due to its sensibility to defects, traps or generation-recombination centers, LF noise is proposed as a good tool to predict the reliability of devices, and to probe technological processes that produce better quality films with less defects. Moreover, LF noise spectroscopy is a non destructive characterization technique. First of all we will present some general aspects of LF noise: the basic of electrical transport fluctuations, the interest of this technique to probe defects in materials and components. Then the LF noise measurement technique used to test bipolar transistors will be introduced. The last section will be devoted to the location of the LF noise sources in the different advanced bipolar transistors studied (BiCMOS technologies developed by STMicroelectronics), by studying the influence of some technological parameter on the LF noise. In particular we will bring to the fore the role of the polycrystalline-silicon/monocrystalline-silicon interface in the neutral emitter layer on the 1/f noise behavior and of the carbon content of the SiGeC base epitaxial layer as active electrical defects. Finally, it is shown that LF noise spectroscopy is a good tool to propose a physical understanding of the trapping/detrapping mechanism and to study the effects of electrical stress on transistors.

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(close full abstract)

16:30

Transmission electron microscopy study of the platinum germanide formation process in the Ge/Pt/SiO2/Si structure

Authors : A. Łaszcz[1], J. Ratajczak[1], A.Czerwinski[1], J. Kątcki[1], V. Srot[2], F. Phillipp[2], N. Breil[3,4], G. Larrieu[3], E. Dubois[3] [1] Institute of Electron Technology, Al. Lotników 32/46, 02-668 Warsaw, Poland [2] Max-Planck-Institut für Metallforschung, Heisenbergstr. 3, D-70569 Stuttgart, Germany [3] IEMN/ISEN, UMRS CNRS 8520, Avenue Poincare, Cite Scientifique, BP 69, 59652 Villeneuve d' Ascq Cedex, France [4] STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France

Resume : Platinum silicide is a very attractive material as a band-edge source/drain for p-type MOSFETs. However, during silicidation of platinum, entire metal layer is not transformed into silicide. The excessive Pt should be removed, without affecting the already formed silicide. Since the only existing selective etchant - aqua regia - etches also silicide, an alternative solution has been proposed. This solution consists in the transformation of the excessive Pt into more reactive Pt-Ge phases, which are easily etched in a sulfuric peroxide mixture. Hence, the mechanisms of the platinum germanide formation in the Ge/Pt/SiO2/Si structure have been studied. Platinum germanide has been formed by the solid-state reaction between Ge (45 nm) and Pt (20 nm) layers during the RTA process within a range of temperatures from 200 to 600 °C. The studies have been focused on TEM observation of the layer microstructure, and Ge/Pt interfaces in an atomic scale (HRTEM), as well as the identification of formed phases using analytical TEM and diffraction techniques. TEM results shows that after annealing at 300 °C the germanidation reaction is already completed. Different Pt-Ge phases have been found in studied samples. The phase composition depends on annealing temperature and the Ge content in the Pt-Ge phases increases with temperature. Analytical and diffraction TEM results have been correlated with XRD measurements.

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(close full abstract)

16:30

EFFECT OF ANNEALING UNDER STRESS ON STRUCTURE OF Si-Ge

Authors : A.Misiuk, Institute of Electron Technology, 02-668 Warsaw, Poland; N.V.Abrosimov, Institute of Crystal Growth, Berlin, Germany; J.Bak-Misiuk, P.Romanowski, Institute of Physics, PAS, Warsaw, Poland; A.Wnuk, W.Wierzchowski, B.Surma, Institute of Electronic Materials Technology, Warsaw, Poland; K.Wieteska, Institute of Atomic Energy, Otwock, Poland; W.Graeff, HASYLAB at DESY, Hamburg, Germany

Resume : Single crystalline 111 oriented Si-Ge samples, grown by a Czochralski method, with Ge content, x = 0.014- 0.026 and oxygen concentration 5x10(17)cm(-3), were processed for 5 h at 1270 K / 1400 K (HT), under pressure 10(5) Pa or 1.2 GPa (HP). Structure of Si-Ge was determined by synchrotron topography, high resolution X-ray diffractometry, Infrared Spectrometry and photoluminescence (PL) measurements. Topography of Si-Ge reveals growth bands, related to Ge segregation; the presence of dislocations at 10(3)cm(-2) density, decorated at HT–HP, has been stated. X-Ray diffuse scattering was most pronounced for the sample with x=0.026; its intensity decreased with HT (HP). Processing at 1270 K resulted in increased lattice parameter, e.g. for Si-Ge (x=0.018), a=0.5441567 nm while 0.5441009 nm only for the as grown sample. Intensity of PL at about 1.07 eV, related to the presence of electron hole droplets (EHD), decreases after processing of Si-Ge at HT–(HP) also evidencing out-annealing of point-like defects, especially under HP.

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(close full abstract)

16:30

E center annealing in SiGe: Stability and charge states

Authors : K. Kuitunen, S. Kilpeläinen, J. Slotte, and F. Tuomisto Laboratory of Physics, Helsinki University of Technology, P.O. Box 1100, FI-02015 TKK, Finland

Resume : We have studied proton irradiated and annealed n-type SiGe with a P dopant concentration in the 1×1018 cm-3 range by positron annihilation spectroscopy (PAS). The Ge contents in the samples were 10, 20 and 30%. The results show that by annealing the irradiated samples at temperatures 275-325 ºC, the Ge content around the E center increases. A step like change in the Doppler broadening parameter S is observed when the measurement temperature is decreased. In addition, the coincidence measurements of the Doppler broadening suggest that the

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positron localization at the E center is significantly stronger at low temperatures. These observations indicate that a charge transition into a more negative state takes place in the upper half of the band gap. According to previous studies, the acceptor level of the E center should be in the lower half of the band gap in 30 % SiGe and thus undetectable with PAS in n-type samples. Hence, we suggest that the increase in Ge content around the E center pulls down the localized second acceptor state, found in Ge, into the SiGe band gap. This charge transition is still observed in samples with 30% Ge, annealed with a considerably higher thermal budget than expected for the complex to anneal completely.

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(close full abstract)

16:30

High-concentration diffusion profile modelling of low-energy ion-implanted B and BF2 in silicon : study of fluorine effect on boron diffusion

Authors : J. Marcon, Université de Rouen, Laboratoire Electronique Microtechnologie et Instrumentation, France A. Merabet, Université de Sétif, Laboratoire de Physique et Mécanique des Matériaux Métalliques, Algérie

Resume : We have simulated the boron-enhanced diffusion (BED) and the transient enhanced diffusion (TED) of boron implanted in silicon following the model proposed by M. Uematsu. We have used published data for B implantation with an energy of 500 eV. This paper investigates how the thermal diffusion of boron is influenced by fluorine implant. Several alternative mechanisms have been proposed to explain the effect of the fluorine on both boron transient enhanced diffusion and boron thermal diffusion in silicon. Interaction between boron and fluorine has been studied to explain the suppression of boron transient enhanced diffusion by fluorine in which the fluorine combines with interstitial boron reducing its mobility. Alternatively, the formation of vacancy-fluorine complexes could be proposed which act as a barrier for boron diffusion. Finally, the interaction of fluorine with silicon interstitials could be also proposed as a mechanism of suppressing boron transient enhanced diffusion. Published experiments have been performed to investigate how the fluorine implantation dose influences the thermal diffusion. Consequently, the fluorine effect on boron diffusion in silicon is still an open question and this paper is a contribution to obtain a satisfactory boron diffusion model in silicon.

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(close full abstract)

16:30

Segregation of antimony to Si/SiO2 interfaces

Authors : Christian Steen,1, Peter Pichler,2,1 Heiner Ryssel,1,2 1 Chair of Electron Devices, University of Erlangen-Nuremberg, Cauerstrasse 6, 91058 Erlangen, Germany. 2 Fraunhofer Institute of Integrated Systems and Device Technology (IISB), Schottkystrasse 10, 91058 Erlangen, Germany.

Resume : Segregation of n-type dopants to interfaces is an important contribution to the loss of electrical activity in current and future device generations. In this work, the segregation and pile-up of antimony atoms at the Si/SiO2 interface in steady state was investigated at a temperature of 1000 °C by a combination of gracing incidence x-ray fluorescence spectroscopy (GI-XRF) measurements, electrical measurements, and etching on the nanometer scale. The antimony atoms were implanted with energies of 10 and 50 keV. The higher energy had the aim to separate the surface segregation clearly from cluster formation around the projected range of the implanted ions. Because of inherent limitations in the GI-XRF analysis of antimony, the investigation had to be restricted to implant doses from 1E14 to 3E15 cm-2. Long annealing times were used to make sure that the segregated atoms are in steady state with the antimony atoms in the bulk. By GI-XRF measurements and removal of the highly doped segregation layer by a sensitive etching process it is possible to distinguish clearly between the piled-up atoms and the antimony atoms in the bulk. The concentration of the latter was obtained from the sheet concentration of arsenic removed by an anodic oxidation. Assuming that the segregated atoms are electrically neutral, their sheet concentration can be described quantitatively via a steady state with positively charged substitutional antimony atoms and free electrons.

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16:30

Simulation of Dopant Diffusion and Activation during Flash Lamp Annealing

Authors : D. Matveev, C. Zechner, N.Zographos Synopsys Switzerland LLC, Affolternstrasse 52, CH-8050 Zurich, Switzerland W. Lerch, S. Paul Mattson Thermal Products GmbH, Daimlerstrasse 10, D-89160 Dornstadt, Germany

Resume : A set of advanced models implemented into the simulator Sentaurus Process was applied to simulate ultra-shallow junction formation by flash lamp annealing (FLA). The full path transient enhanced diffusion model includes equations for small interstitial clusters (I2, I3, I4), {311} defects and dislocation loops. The dopant-point defect clustering model is used for dopant activation simulation. Several cluster types are considered: B2, B2I, B2I2, B3I, B3I2, B3I3 for boron and As2, As2V, As3, As3V, As4, As4V for arsenic. Different point defect and dopant-point defect pair charge states are taken into account to obtain accurate results in the high doping level region. The FLA process was performed at various peak temperatures in Mattson Millios fRTP system. The measured wafer temperature as a function of time allowed us to simulate the transient processes with a high accuracy. A good agreement between SIMS and simulated profiles was achieved. The sheet resistance dependence on the FLA peak temperature was reproduced successfully.

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16:30

On the activation mechanisms of sub-melt laser anneals

Authors : T. Clarysse (a), J. Bogdanowicz (a), J. Goossens (a), A. Moussa (a), E. Rosseel (a), W. Vandervorst (a,b), D.H. Petersen (c,d), R. Lin (d), P.F. Nielsen (d), O. Hansen (c,e), C. Defranoux (f), A. Vertikov (g), M. Gostein (g), N.S. Bennett (h), N.E.B. Cowern (h), V.N. Faifer (i), (a) IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, (b) K.U.Leuven, IKS, Department of Physics, Celestijnenlaan 200D, B-3001 leuven, belgium, (c) MIC, Department of Micro and Nanotechnology, NanoDTU, DTU, b-345 East, DK-2800 Kgs. Lyngby, Denmark, (d) CAPRES A/S, Scion-DTU, Building 373, DK-2800 Kgs. Lyngby, Denmark, (e) CINF, Centre for Individual Nanoparticle Functionality, NanoDTU, DTU, b-345 East, DK-2800 Kgs. Lyngby, Denmark, (f) SOPRA, 26 rue Pierre-Joigneaus, F 92270 Bois-Colombes, France, (g) AMS, Advanced Metrology Systems LLC, 12 Michigan Drive, Natick MA 01760, USA, (h) School of Electrical, Electronic and Computer Engineering, University of Newcastle upon Tyne, Newcastle upon Tyne NE1 7RU, UK, (i) Frontier Semiconductor, 199 River Oaks Parkway, San Jose, CA 95112, USA

Resume : In order to fabricate carrier profiles with a junction depth (~15 nm) and sheet resistance value suited for sub-32 nm Si-CMOS technology, the usage of sub-melt laser anneal is a promising route to explore. Whereas laser annealed junctions outperform standard anneal approaches, the basic mechanisms of laser induced activation are not yet clear. In this work we study the activation behavior of low and high concentration levels (i.e. below and above solid solubility) as well as their concurrent mobilities. The parameters included in this study are the concentration range, the presence/absence of a PAI-implant as well as the role of different sub-melt laser anneal treatments
(dwell times of 0.25-1.5 ms). Activation levels are extracted from a comparison between the dopant 8
profiles as measured by Secondary Ion Mass Spectrometry, and the activated fraction as extracted 11
from sheet resistance and mobility measurements. The latter are based on a large variety of techniques. For the sheet resistance we use medium (cm) and high resolution (mm) contactless RsL, micro four point probe and optical techniques such as Infra-Red Spectroscopic Ellipsometry and Model Based Infra-Red (IRSE, MBIR) measurements. For the mobility extraction we use conventional Hall, IRSE and MBIR, and a recently developed new Hall-like capability using the micro four point probe.

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(close full abstract)

16:30 p+ poly gate formed by the B18H22 ion implanted compensation on the in situ phosphorus (n+) doped poly silicon gate

Authors : Wei-Chiang Lee, J. Hwang** Department of Material Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan 300, ROC

Resume : Dual poly gate CMOS is essential for the low-voltage operation because low threshold voltage p-channel MOSFET can not be made by buried channel but surface channel. B18H22 cluster
ion implantation has higher throughput compared with traditional B ion implantation. B18H22 8
cluster ion implantation was applied using various energy and dosage to change in-situ n+ into p+ 12
poly gate for throughput improvement. Experimental results indicate that the projected range defects (PRDs) make boron difficult to diffuse into the bottom of the in-situ n+ poly gate, resulting in lower boron concentration near the bottom of the poly gate. Both secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP) were used to measure the boron distribution and the sheet resistance in gate poly after annealing in order to determine the optimum implantation conditions.

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(close full abstract)

16:30 Phosphorous clustering in germanium-rich silicon germanium

Authors : A. Chroneos1, R. W. Grimes1, B. P. Uberuaga2, H. Bracht3 1Department of Materials, Imperial College London, London SW7 2BP, United Kingdom 2Materials Science and Technology Division, Los Alamos National Laboratory, Los Alamos, New Mexico 87545, USA 3Institut für Materialphysik, Universität Münster, Wilhelm-Klemm-Strasse 10, D-48149 Münster, Germany

Resume : The formation of clusters consisting of donor atoms and lattice vacancies can deleteriously affect the performance of silicon germanium devices. In the present study results from
electronic structure calculations are evaluated using mass action analysis to identify the extent to 8
which phosphorous-vacancy clusters form in germanium-rich silicon germanium. Although it is 13
energetically favourable to form clusters containing up to four phosphorous atoms, clusters are only important at lower temperatures. At such temperatures the formation of the cluster in which four phosphorous atoms are tetrahedrally coordinated around a vacancy is especially important. The formation of the larger clusters might be hindered by kinetic effects and for this reason the relative concentrations of the mobile phosphorous-vacancy pair and the two phosphorous-vacancy cluster are particularly important as they act as precursors for the formation of the larger clusters. At high temperatures unbound vacancies and phosphorous atoms are dominant.

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(close full abstract)

16:30 Impact of fluorine co-implantation on B deactivation and leakage currents for low and high energy Ge preamorphised p+n shallow junctions

Authors : D. Girginoudi and C. Tsiarapas Department of Electrical and Computer Engineering, Democritus University of Thrace, 67100, Xanthi, Greece

Resume : The impact of fluorine co-implantation on boron deactivation and boron TED, as well as on the I-V characteristics of p+n diodes, have been studied for low (10 keV) and high (70 keV) Ge preamorphised n-type silicon samples, that annealed at 600 0C and 700 0C. Transmission electron microscopy revealed the existence of <311> defects and dislocation loops in the EOR region. It has been found that F stabilizes the EOR defect population via the increase of EOR defect density and the percentage of the stable dislocation loops. This phenomenon is more pronounced when the preamorphisation is shallow (10 keV Ge energy). SIMS and sheet resistance measurements showed that boron forms clusters (BICs) with silicon interstitials released from EOR region, especially in the shallow preamorphised samples and at the 700 0C annealing temperature. The existence of BICs
implies boron deactivation, while other interstitials affect boron diffusivity, increasing boron TED. 8
The role of fluorine on boron deactivation is multilateral: At the 70 keV preamorphised samples and 14
at 600 0C annealing temperature, fluorine forms clusters with boron causing further boron deactivation. At the 700 0C annealing case, fluorine probably forms Fluorine-Vacancy (F-V) clusters that trap the silicon interstitials, reducing the possibility of forming BICs and, therefore, resulting in boron re-activation and suppression of boron TED. At the 10 keV preamorphised samples, and irrespectively of the annealing temperature, F improves significantly the sheet resistance, and we suggest that this is a result of two contributing physical mechanisms: i) In the EOR region, F is trapped into dislocation loops, which release less silicon interstitials than other types of defects. ii) In the amorphous part of silicon, there are probably F-V clusters that trap the silicon interstitials released from the EOR region. Although F improves boron deactivation in most cases, it increases the reverse leakage currents, probably due to the stabilization of the defects in the EOR region. Regarding the carrier-transport mechanisms, it has been found that the dominant mechanism is the generation-recombination process at the forward-bias as well as at the larger part of the reverse bias voltage regions.

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16:30

INTERACTIONS AND CLUSTERING OF COBALT ATOMS IN SILICON

Authors : M.G. Ganchenkova 1, V.A. Borodin 2, F. Fortuna 3, M.-O. Ruault3, and R.M.Nieminen 1 1 Helsinki University of Technology, P.O.Box 1100, 02015, Espoo, Finland, 2 RRC Kurchatov Institute,

123182 Moscow, Russia 3 CSNSM, Univ. Paris-Sud, bat. 108, 91405, Orsay, France
Resume : A promising modern way of nano-engineering involves the use of ion beam synthesis, which starts from the nucleation and growth of nanosize precipitates, and may further include cluster coalescence and formation of continuous buried layers. In particular, IBS is widely used for creation of cobalt disilicide nanostructures, which are attractive for use in microelectronics applications due to their specific properties, such as low electrical resistivity and high-temperature stability. The efficiency of cobalt disilicide precipitation and the shapes of the forming clusters are highly sensitive to the nucleation environment, being quite different in the thermal annealing and ion implantation conditions. The formation of disilicide cluster nuclei, which determines the subsequent precipitate kinetics, can be properly understood and simulated only provided one knows correct energies for metal atom diffusion and binding. Moreover, since ion implantation creates noticeable amounts of Frenkel pairs, it is important to know the energetics of cobalt interaction with intrinsic point defects.. Unfortunately, the database of the solution energies of differently charged Co atoms in silicon, as well as of Co atom interaction energies between themselves and with radiation defects is fragmentary (see e.g. [1]). In this report we present the equilibrium configurations and formation energies of various small clusters of cobalt atoms and vacancies calculated in the framework of the density functional technique with explicit account for electron spins and d-electron shells of Co atoms. It is shown that certain configurations of small interstitial Co clusters lead to spontaneous bond reordering of surrounding Si atoms and the formation of chemically bound Co-Si clusters, while interaction of interstitial cobalt atoms with vacancies can result in cluster nuclei with twinned alignment with respect to the host silicon lattice. The application of the obtained data for lattice kinetic Monte-Carlo modeling of cluster formation during high-temperature annealing provides for the first time the explanation how proper CoSi2 particles (with Co atoms on fcc sublattice) form from Co interstitials diffusing on diamond-like sublattice of interstitial sites in the bulk Si. References: [1] R.Stadler, R.Podloucky, G.Kresse, J. Hafner, Phys. Rev. B 57, 4088 (1998).

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16:30

E-CENTERS IN STRAINED SILICON

Authors : S. Nicolaysen 1, M.G. Ganchenkova 2 and R.M. Nieminen 2 1 Institute for Microsystem Technology, P.O.Box 2243, N-3103 Tonsberg, Norway 2 Helsinki University of Technology, P.O.Box 1100, 02015, Espoo, Finland,

Resume : The application of strained silicon in microelectronics is prompted by significant improvements in device performance and functionality that can be reached by replacing bulk, cubic-crystal Si wafer with a tetragonally distorted, biaxially strained Si layer grown epitaxially on other substrates with different lattice parameter. Both the electronic band structure and the properties of localized levels associated with defects in Si are affected by elastic strains. Moreover, the non-hydrostatic strains noticeably change the magnitudes of defect formation, migration and interaction energies, making them sensitive to the applied stress orientation with respect to the lattice. Among the most critical defects for silicon technology are vacancies and small vacancy-impurity clusters (such as E-centers, e.g. As-V and Sb-V pairs). Although in relaxed Si the defect formation energies and electronic structure are thoroughly investigated using powerful approaches (such as density functional technique), not much is known about the effect of elastic strain on these properties. Here we investigate first of all the effect of non-hydrostatic stress on the vacancy interaction with an impurity atom (As or Sb) in silicon at separations up to the third nearest neighbours. The total energies of vacancy-impurity pairs at different pair orientations were calculated using the first-principles approach. It is demonstrated that the energy of a vacancy-impurity pair is indeed sensitive to the pair orientation with respect to the direction of applied stress. The stress-induced changes of the vacancy-impurity pair energies with respect to the relaxed Si depend on the pair charge and can reach several tenths of eV at strains ~1% (or stresses close to 1 Gpa). It is found that the application mode and the magnitude of elastic strain noticeably influence the presence and positions of localized levels introduced by vacancy-impurity pairs into the band gap. The defect formation energies are demonstrated to vary linearly with strain for strains smaller than 1%. The linear range of energy-strain dependencies is used for the estimation of vacancy-impurity pair dipole tensors.

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16:30

Internal Mechanical Stresses and Strain Relaxation in the Si-SiO2 system.

Authors : D. Kropman, E. Mellikov, O. Volobujeva Tallinn University of Technology (Estonia) Ü. Ugaste, T. Laas Tallinn University (Estonia) I. Heinmaa Institute of Chemical Physics and Biophysics (Estonia) A. Medvid Riga Technical University (Latvia)

Resume : It is known that internal mechanical stresses due to the differences in the thermal expansion coefficient between films and substrates and lattices mismatch appear in the Si-SiO2 system during the process of its formation and that point defects generation and redistribution reduce partially the surface strain. However,no investigation of this procsess on the atomic scale has been carried out so far. The purpose of the present work is to investigate the strain relaxation mechanism in the Si-SiO2 system by means of EPR, IR absorption spectroscopy, scanning elektron microscopy (STM) and samples bending measurements. It has been found that samples bending increases or decreases with EPR signal intensity depending on the oxidation temperature and oxidation time. It may be due to the relaxation of strain by the point defects, and to the creation of point defects by the stresses.The dependence of the EPR signal (I) on the oxidation time reveal one or two maxima depending onthe cooling rate. In fast-cooled samples there exist a correlation between I and IR absorbtion linewidth at 1100cm-1(Δv). In slowly cooled samples the decrease of the EPR signal is accompanied by the increase of the Δv value. This can be explained by the influence of the vacancies on the thermal expansion of Si. This can occur due to diminishing of the internal mechanical stresses as a results of the opposite sign of thermal expansion coefficient of SiO2 and Si3N4 on Si. After Si3N4 deposition samples bending cheing sign and instead the tensil stresses, compressiv stresses appear at the interface.

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(close full abstract)

16:30

Diffusion of phosphorus implanted in germanium

Authors : Thomas Canneaux(1), Daniel Mathiot(1), Jean-Pierre Ponpon(1), Stephane Roques(1), Sebastien Schmitt(1), Christiane Dubois(2). 1- InESS, BP 20 CR, F 67037 Strasbourg Cedex 2, France. 2- INL Institut des Nanotechnologies de Lyon, INSA de Lyon, 7 avenue Capelle, F-69621

Villeurbanne Cedex, France. e-mail: thomas.canneaux@iness.c-strasbourg.fr
Resume : Presently, the majority of integrated circuits and electronic devices are made with silicon. But, according to ITRS, it will be difficult to follow Moore\\\\\\\'s law in a few years with Si devices. Today, several ways are possible to continue to improve electronic device performances and speed. For most of them, a complete change of methods to produce electronic devices is needed. But, there is one way in which there will not have to be any change in the fabrication processes of electronic devices; this is by using germanium. Until now, Ge has not really been used for electronic devices mainly because its oxide is volatile, in contrary to SiO2 used in fabrication of electronic devices as dielectric. But, to follow Moore\\\\\\\'s law with silicon, it is necessary to change the dielectric, and so, Si loses its best advantage against Ge, in which careers have a higher mobility. There are some study about dopant diffusion in Ge, most of them was done in 50\\\\\\\'s and 60\\\\\\\'s and are not accurate enough and influence of some recent techniques was not studied. Here, we discuss about our experimental protocol to study diffusion of boron, phosphorus, arsenic and gallium in germanium. To carry out our experiments, we make a deposition of amorphous germanium on a germanium monocrystalline, implant an accurate quantity of dopant in this amorphous layer, make an anneal to recrystallize this layer and an other to perform diffusion of dopant. We study this diffusion by SIMS measurements. 8 18

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(close full abstract)

16:30 Boron Activation in SOI and strained-SOI after 1 keV B+ ion implantation and
Authors : D. Buca, F. Lanzerath, J.Knoch, S. Mantl Institute of Bio- und Nanosystems and cni – Center of Nanoelectronic Systems for Information Technology, Forschungszentrum Jülich GmbH, D-52425 Jülich, Germany U. Breuer Zentralabteilung für Chemische Analysen, Forschungszentrum Jülich GmbH, D-52425 Jülich, Germany W. Skorupa Institute of Ion Beam Physics and Materials Research, FZ Rossendorf, 01328 Dresden, Germany B. Ghyselen SOITEC, Parc Technologique des Fontaines, 38190 Bernin, France
Resume : For the formation of ultra shallow junctions for the 45nm CMOS node and beyond millisecond annealing is most promising. In this work, SOI and strained SOI wafers were implanted with B+ at a low energy of 1 keV and doses of 1E14, 1E15 and 1E15 cm-2. The thermal activation was achieved using a flash pulse with duration of 3 ms after the sample was preheated to a temperature of 650°C. For comparison standard RTP annealed samples were 1prepared. Dopant diffusion was investigated by SIMS. None of the investigated flash lamp annealed samples showed any dopant redistribution, even at highest flash energy. Hall measurements showed a high activation in both, SOI and sSOI, comparable to the RTP samples. However, boron activation of sSOI appeared usually lower than that of SOI mainly due to the higher reflectivity of sSOI. In order to improve the absorption characteristics we computed the optical properties of the heterostructures after adding a SiO2 antireflection layer. Based on these estimates a 240nm thick SiO2 layer was deposited on both, SOI and sSOI. As an effect a decrease of □60% of the layer sheet resistance and an increase of □200% of the doping activation for sSOI is obtained. We will show that flash lamp annealing outperforms standard RTP for the formation of ultra-shallow junctions with negligible diffusion and sheet resistance as low as 306 Ω/square for SOI, which is comparable with results achieved on bulk silicon. 8 19

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(close full abstract)

16:30 Impact of Inactive Dopants in Chemical Vapor Deposition Layers on Photomodulated Optical Reflectance
Authors : Janusz Bogdanowicz (a,b,1), Fabian Dortu (a,b), Trudo Clarysse (a), Wilfried Vandervorst (a,c), Derrick Shaughnessy (d), Alex Salnik (d), Lena Nicolaides (d) (a) IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (b) Electrical Engineering Department, INSYS, KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium (c) Instituut voor Kern- en Stralingsfysika, KU Leuven, B-3001 Leuven, Belgium (d) KLA-Tencor Corp., 160 Rio Robles San Jose, California 95134 (1)E-mail: Janusz.Bogdanowicz@imec.be
Resume : The ITRS roadmap stresses the electrical characterization of the active doping profiles for sub-30 nm structures as a key challenge for future CMOS technology. Presently, there is no technique satisfying the ITRS targeted depth (3%) and carrier level (2%) reproducibility and accuracy. Earlier work has shown the promising capabilities of non-destructive Photomodulated Optical Reflectance (PMOR) techniques, based on the localized detection of variations in the reflectivity of the sample, due to thermal and plasma (excess carrier) effects as can be generated by a modulated pump laser such as the Therma-Probe® (TP) system. In particular, a single measurement has shown to allow for the direct extraction of the junction depth and carrier concentration of box-like carrier profiles. However, attempts to model quantitatively the PMOR signals on such layers have failed up to now. In this work, we study the impact of the inactive dopant atoms in Chemical Vapor Deposition (CVD) layers. We first give evidence for the partial inactivation of the CVD layers by means of a comparison between Four-Point Probe, Secondary Ion Mass Spectrometry and Spreading Resistance data. We then investigate its impact on the PMOR signals. In particular, with the help of numerical simulations, this work shows that, by taking into account the combined degradation of the thermal conductivity and of the recombination lifetime, the theory may be rendered quantitative. 8 20

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16:30

Carbon Effect on Electrical Characteristics of Hight Speed SiGeC HBT
Authors : Maya LAKHDARA 1, Saïda LATRECHE 1, José Cruz NUNEZ-PEREZ 2, Manel BOUHOUCHE 1, J. VERDIER 2 and Christian GONTRAND 2 (1) Laboratoire Hyperfréquence & Semi-conducteur (LHS), Département d'Electronique Faculté des Sciences de l'Ingénieur, Université Mentouri, Constantine, 25000, ALGERIA. Tel /Fax: + 213 31 81 68 89 l_maya1@yahoo.fr, slatrech@yahoo.fr (2)INL, Institut des Nanotechnologies de Lyon, INSA- Lyon, CNRS. Bâtiment Blaise Pascal, 7 avenue Jean Capelle Villeurbanne Cedex F-69621, FRANCE christian.gontrand@insa-lyon.fr Tel /Fax: +33 4 72 43 80 67/ +33 4 72 43 60 81
Resume : In order to meet the demands of the explosive spread of high speed and mass data telecommunications, SiGe:C Herojunction Bipolar Transistors (HBTs) are being investigated. Although a large amount of Ge in the SiGe base improves the figures of merit of HBTs, the devices suffer from a lot of problems. First, in SiGe/Si devices the exodiffusion of Boron (B) across the junctions deteriorates devices performances. Next, the large lattice mismatch between Si and Ge in the SiGe base reduces the value of critical thickness affecting the stability of the base film. The

incorporation of carbon (C<1%) in the SiGe base prevents the auto-diffusion of B across the junctions, improves the film stability by reducing strain, and leads to better process integration. Addition of carbon in the base layer of SiGe HBTs has been reported as an effective way to achieve high-performance devices. This paper analyses a SiGeC HBTs, with and without carbon, using our device simulator Sibidif. We present a numerical modelling of a NPN (SiGeC) HBT realized in an industrial BiCMOS SiGe:C 0,13µm-like process, taking into account the effect of an incorporation of a small amount (0.5%,0.75%,1%) of carbon in the HBT device. "SIBIDIF" is a two dimensional Drift –Diffusion Model (DDM) simulator. It solves the continuity equations for electrons and holes, coupled with the Poisson's equation, based on the concept of the finite difference mesh. Current gain seems to decrease continuously with the increase of carbon concentration. The results obtained in this study are efficiently compared with electrical characteristics obtained by measurements and SPICE-like parameter extractions from simulations via a compact model (HICUM) implemented in the so-called commercial simulator ADS (Advanced Design System) . Nevertheless, the electric performances of this device can be penalized by the presence of defects inherent to the complex structure shrinking. Then, we focused on the defect's identification responsible for the current fluctuations at the origin of low frequency noise or Random Telegraphic Signals in industrial submicronic BiCMOS technologies. Gummel characteristics are simulated in order to identify generation-recombination or trap assisted tunnelling process in the base current. We have shown that devices having an excess base current present random discrete fluctuations on the base current.

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16:30

Thermal Stability of Ni-Pt and Ni-Pt-Ta Alloy Silicides Formed on epi-Si1-xCx

Authors : Jung-Ho Yoo1, Hyun-Jin Chang1, Mann-ho Cho2, Tae-Wan Lee3 and Dae-Hong Ko1 1. Department of Ceramics Engineering, Yonsei University, Seoul 120-749, Korea 2. Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea 3. Jusung Engineering Co., Ltd., 49, Neungpyeong-ri, Opo-eup, Gwangju-Si, Kyunggi-do, Korea, 464-892, Korea

Resume : As scaling down, the conventional devices came to have some issues like the decrease of channel mobility originated from the increase of leakage current. To enhance the CMOS performance, channel strain engineering by lattice mismatch has been widely introduced. Recently, to improve the channel mobility for NMOS, many researches about S/D epi-Si1-xCx which induces tensile strain at the channel are in progress. In order to apply epi-Si1-xCx in S/D regions, the application of silicide process should be considered and optimized. Among various metal silicide candidates, Ni silicide is a promising material due to its low resistivity, low silicidation temperature, less Si consumption, and line-width independency. However, NiSi shows morphological and electrical instabilities for additional heat-treatment after the SALICIDE process. The instability of NiSi film is attributed mainly to transformation from NiSi to NiSi2 during post heat-treatment. Recently, it was reported that the addition of a small amount of Pt into Ni enhanced phase stability. Also, many other Ni-alloy materials have been considered as a promising silicide to enhance the thermal stability. We investigated the formation and the thermal stability of Ni-Pt and Ni-Pt-Ta silicides on epi-Si1-xCx in order to apply these films to the gate-source-drain region of the ULSI device. Epi-Si1-xCx films with various carbon contents were deposited by UHVCVD on Si(100). After the removal of the native oxide, 20 nm thick Ni-Pt and Ni-Pt-Ta alloy films were deposited by direct DC magnetron sputtering. The Ni-silicide films were formed by rapid thermal annealing process in N2 ambient. The resulting films were analyzed and compared by four-point probe, RBS, XRD, HR-TEM, and SIMS.

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16:30

Activation and diffusion studies for boron ultra shallow junctions in Silicon after non-melting Excimer laser annealing

Authors : A. Florakis1, N. Misra2, C. Grigoropoulos2, D. Tsoukalas1,3, K. Giannakopoulos4, A. Halimaoui5 1 Department of Applied Physics, School of Applied Sciences, National Technical University of Athens, 9 Heroon Polytechniou Str.,15780 Zographou, Greece 2 Department of Mechanical Engineering, University of California Berkeley, 6177 Etcheverry Hall CA 94720-1740 3 Institute of Microelectronics, NCSR Demokritos, 15310 Aghia Paraskevi, Greece 4 Institute of Materials Science, NCSR Demokritos, 15310 Aghia Paraskevi, Greece 5 ST Microelectronics, 850 rue Jean Monnet, 38926 Crolles cedex, France

Resume : Following previous studies using Excimer laser at fluencies above melting threshold, in the current work we present results on mon-melting Excimer laser annealing in order to obtain difussionless activation of Boron for the creation of Ultra Shallow P-MOS devices. In order to fulfill the strict requirements imposed by the ITRS roadmap for the 32 nm node we have implemented two emerging techniques; non-melt laser annealing and BF3 plasma doping implantation (PLAD). The later leads to the creation of ultra shallow and abrupt as implanted profiles (χj less than 13 nm, abruptness<2.5nm/decade). On the other hand, with the use of non-melt laser annealing, we can obtain high level of electrical activation, while practically eliminating Boron diffusion, due to its capability to deliver low thermal budget in the nanosecond time scale. An Excimer KrF laser (λ=248nm and pulse duration 38ns) has been used for the irradiation. In order to determine the optimum annealing conditions in terms of low junction depth and sheet resistance values, and damage annihilation, we have performed a variety of annealing conditions regarding the energy density and the number of pulses. The post annealing characterization of the samples included Secondary Ion Mass Spectroscopy and Van Der Pauw Sheet resistance measurements. SIMS data indicate difussionless dopant behavior with Rs values at 600Ω/sq. We have concluded our analysis with the examination of the morphological characteristics both of the surface of the sample (using Atomic Force Microscopy) and the evolution of the recrystallization of the amorphised layers and the removal of the defects (by means of cross-section Transmission Electron Microscopy).

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16:30

Fluorine effect on B electrical activation in Si

Authors : G. Impellizzeri, S. Mirabella, A. M. Piro, M. G. Grimaldi, F. Priolo MATIS CNR-INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, ITALY F. Giannazzo, V. Raineri CNR-IMM, Sezione di Catania, Stradale Primosole 50, 95121 Catania, ITALY E. Napolitani, A. Carnera MATIS CNR-INFM and Dipartimento di Fisica, Università di Padova, Via Marzolo 8, 35131 Padova, ITALY

Resume : During the last years F has attracted the interest of the microelectronic community for

its efficiency in reducing the B diffusion in Si. If on one hand small junction-depth extensions are necessary for scaling down Si devices, on the other hand holding low values of sheet resistance is necessary too. In this work we focused on the latter issue, investigating the effect of F on the electrical activity of B-doped junctions. We studied pre-amorphized Si samples, implanted with B and/or with F and finally re-grown by solid phase epitaxy. Hall effect and four-point probe analyses with the Van der Pauw method showed a significant loss of carrier dose of about 15% in the B-doped junction enriched with F with respect to the sample implanted only with B. In principle, formation of B-F complexes could explain this partial electrical deactivation, however by nuclear reaction analyses, in channeling configuration, we demonstrated that B is fully substitutional also in presence of F. These structural analyses are hence not consistent with the formation of B-F complexes. On the contrary, scanning probe microscopy analyses of the electrical activity of F alone have surprisingly demonstrated, and quantified, a significant n-type doping of F in Si. Our results definitively clarify that the loss of hole dose in junctions co-implanted with B and F is not due to a B-F chemical bond, but simply to a partial dopant compensation effect. 8 24

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16:30 Modelling of Boron Trapping at End-Of-Range Defects in Pre-amorphized Ultra-Shallow Junctions

Authors : E. M. Bazizi, LAAS-CEMES/CNRS–ST Microelectronics, 7 av. Col. Roche, 31077 Toulouse, France; P. F. Fazzini, CEMES-LAAS/CNRS, 7 av. Col. Roche, 31077 Toulouse, France; C. Zechner, A. Tsibizov, Synopsys Switzerland LLC, Affolternstrasse 52, 8050 Zuerich, Switzerland; H. Kheyrandish, CSMA, Queens Road Penkhull Stoke-on-Trent Staffordshire, ST4 7LQ, UK; A. Pakfar, L. Ciampolini, C. Tavernier, STMicroelectronics, 850, rue Jean Monnet, 38926 Crolles Cedex, France; F. Cristiano, CEMES-LAAS/CNRS, 7 av. Col. Roche, 31077 Toulouse, France.

Resume : It is known that in p-n junctions fabricated using pre-amorphizing implants, the tail of the Boron concentration profiles show an anomalous peak in correspondence with the End-Of-Range (EOR) defects. In addition, it is generally accepted that the Boron atoms contained in this so-called “trapping peak” are immobile and electrically inactive. With the progressive reduction of the junction depth, predicted by the ITRS, this phenomenon will become more and more critical, as, in ultra-shallow junctions, both the EORs and the B peaks are located at few nanometers from the surface. In this work, SIMS and TEM analysis were used to investigate the evolution of boron trapping at EOR defects. To simplify the modelling task, Si wafers with a constant boron concentration of 2x1018 cm-3 were implanted with 30 keV Germanium and with a dose of 1015 cm-2 and then annealed at 700, 800, or 900 °C in an N2 ambient for various times. A physical model for the Boron trapping at EOR defects has been developed, which takes into account the geometry of the EOR defects. It is assumed that BI pairs can be captured either by {311} defects or by dislocation loops. It will be shown that the behaviour of the boron trapping peak is strongly controlled by the evolution of {311} defects and that the loops contribution to the trapping mechanism is less pronounced. The complex evolution of the trapping peak as a function of both the annealing time and temperature is accurately reproduced by our model. 8 25

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16:30 Mechanism of fluorine segregation and incorporation during solid phase epitaxy regrowth of pre-amorphized silicon

Authors : M. Mastromatteo, E. Napolitani, D. De Salvador, F. Panciera, A. Carnera MATIS CNR-INFM and Dipartimento di Fisica, Università di Padova, Via Marzolo, 8, I-35131 Padova, Italy. G. Impellizzeri, S. Mirabella, F. Priolo MATIS CNR-INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia, I-95123 Catania, Italy.

Resume : Fluorine has attracted intense interest over the last few years due to its ability in reducing B diffusion in pre-amorphized Si, for ultra-shallow p+/n junction formation in CMOS devices. F is incorporated in crystalline (c) Si during Solid Phase Epitaxy (SPE) regrowth following a complex mechanism, still poorly understood, involving F segregation and diffusion in amorphous (a) Si, and SPE retardation. We have investigated in detail, by using Secondary Ion Mass Spectrometry (SIMS), the evolution of the F chemical profile during SPE of pre-amorphized Si implanted with F, in a wide range of F concentrations and SPE temperatures. We show that the F segregating in a-Si during SPE splits in two components, the first one being a distinctive sharp peak segregated at the a/c interface, and the second one being a diffusing tail in the residual amorphous region. In addition, F incorporated in c-Si and the SPE retardation are shown to be strictly related to the above phenomena and to the temperature. On the basis of the above data, we propose a model based on rate-equations, in which F is assumed to diffuse in a-Si and interact with the defects at the a/c interface. The model satisfactorily simulates the F chemical profiles and the a/c interface motion depth. The above results will be also discussed by considering the recently published data on the structural properties of F incorporated in c-Si and its interaction with point defects. 8 26

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16:30 Self-assembly of nanohills in SixGe1-x/Si heteroepitaxial structure due to Ge redistibution induced by laser radiation

Authors : A.Medvid\'1, P.Onufrijevs1, K.Lyutovich2, M. Oehme2, E. Kasper2, N.Dmitruk3, O.Kondratenko3, I.Dmitruk4, I.Pundyk4 1 Riga Technical University, 14 Azenes Str., Riga, LV-1048, Latvia 2 Universitat Stuttgart, Pfaffenwaldring 47, 70569 Stuttgart, Germany 3 Institute of Semiconductor Physics National Academy of Sciece of Ukraine, 45 Pr.Nauki, 252650, Kyiv-28, Ukraine 4Kyiv National Taras Shevchenko University, Kyiv-03022, Pr.acad.Glushko, 2-1, Ukraine

Resume : For the first time observed self-assembling nanohills induced by irradiation of nanosecond Nd:YAG laser pulses (pulse duration 15 ns, wavelength 1062 nm and power 1MW) in the Si 0.7Ge 0.3/Si heteroepitaxial structures with initially uniform distribution of Ge atoms over the top layer is reported. The Photoluminescence band at 700-800 nm the maximum of which shifting to shorter wavelengths with the increase of the intensity of laser radiation and appearance of the 300 cm-1 Ge-Ge vibration band in micro-Raman spectra are explained by the quantum confinement effect in nanohills. An AFM study of the morphology of irradiated surface has shown formation of particularly-oriented nanohills after laser irradiation of the intensity I=32 MW/cm2. Ellipsometry data confirmed appearance of Ge-rich phase precipitates amounting to 4.6% and 2.1% of the total Ge content induced by laser radiation of intensities I1=32 MW/cm2 and I2=25 MW/cm2, respectively. Formation of the Ge-rich phase is explained by localization of Ge atoms drifting toward the irradiated surface under the thermal gradient due to strong absorption of the laser radiation. 8 27

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16:30 Charge of Self-Interstitials and Boron-Interstitial Pairs as a Function of Doping Concentration

Authors : Wolfgang Windl Department of Materials Science and Engineering, The Ohio State University, Columbus, OH 43210-1178, USA

Resume : The diffusion mechanism of boron has not been understood for a very long time despite considerable research interest, which was fueled among others by the fact that boron can display very strong transient enhanced diffusion. We will discuss the accuracy of previous ab-initio calculations for self-interstitial and boron diffusion in light of recent experimental data by Bracht et al. [Phys. Rev. B 75, 035211 (2007)] and by De Salvador et al. [Phys. Rev. Lett. 97, 255902 (2006)]. We mapped the experimental data onto the activation energy vs. Fermi level representation commonly used to display ab-initio results. In this representation, the experimental results are consistent with each other. Compared to the ab-initio results, we confirm that the activation energy for boron diffusion as a function of the Fermi level agrees well with experiment. For the self-interstitial, we find in line with previous calculations a more severe underestimation of the experimental values, despite using total-energy corrections to compensate for the underestimated theoretical band gap. Since the predicted activation energies not only for boron, but also for other interstitial diffusers is in general predicted much better than the selfinterstitial energies, we discuss the possibility that point-defect interactions and reactions could be the reason for the discrepancy between experiment and theory.

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16:30 Analysis of frequency-dependent interface states in PtSi/p-Si Schottky diodes

Authors : A. Sellai (1)*, Z. Ouennoughi (2) 1. Physics Department, P.O Box 36, Sultan Qaboos University 123, Oman 2. Laboratoire optoélectronique et composants, Département de physique UFAS Sétif Algérie

Resume : Abstract. In this work, PtSi/p-Si Schottky structures have been studied using principally conductance and capacitance measurements under forward and reverse biases over a wide range of frequencies and at several temperatures to yield quantitative information about the interface states. The increase of capacitance at lower frequencies is seen as a signature of interface states, the densities of which are evaluated to be of the order of 1013 eV-1cm-2. The presence of interface states is also evidenced (Fig. 1) as a peak in the conductance-frequency characteristics. The conductance data is used, in particular, to extract the relaxation times of interface states and their energy distribution with respect to the top of the valence band. Fig. 1 Measured Conductance versus frequency in forward bias

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18:30 Structural characterization of strained silicon grown on SiGe buffer layer

Authors : J H Jang1, M S Phen1, A Gerger1, K S Jones1, J L Hansen2, A N Larsen2 and V Craciun1 1 Department of Materials Science and Engineering, University of Florida, Box 116400, Gainesville, FL 32611, USA 2 Department of Physics and Astronomy, University of Aarhus, DK-8000 Aarhus, Denmark

Resume : The microstructure of 50 nm thick strained-Si/Si0.7Ge0.3/graded-SiGe/Si-substrate layers grown by MBE (Molecular Beam Epitaxy) was studied using high resolution X-ray based characterization techniques. The degree of relaxation of the Si capping layer after a thermal anneal at 800 for 30 min was determined using Reciprocal Space Map (RSM) scans recorded around the (113) diffraction plane. However, since a RSM is not suitable when the strain relaxation is very small, X-ray reflectivity (XRR) and omega rocking curves (ω-RCs) were employed for the relaxation study. XRR spectra were collected and analyzed to obtain thickness, Ge concentration and surface/interfacial roughness information of the as-grown and annealed samples. ω-RCs were collected and fitted to asses the crystalline quality of the samples. It was found that the annealed strained layer showed higher Lorentzian fraction in ω-RCs and misfit defect density which were caused by strain relaxation. In addition, the results showed that after the annealing process the broadening in the tail region of the ω-RCs was indicative of a change in the coherence length distribution of the crystallite size. The misfit defects and surface morphology obtained from transmission electron microscopy (TEM) and atomic force microscopy (AFM) investigations were consistent with results obtained from the X-ray based characterization techniques.

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PROGRAM VIEW : 2008

MY PROGRAM : 2008

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Front-end junction and contact formation in future Silicon/Germanium based devices

26 May 2008 | 27 May 2008 | **28 May 2008** | 29 May 2008 | 30 May 2008

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start at	Subject	Num.
	Joint Session with Symposium J on Junction Formation in Germanium : Hartmut Bracht, University of Münster	
08:30	Defect Engineering Aspects of Advanced Ge Process Modules Authors : C. Claeys (1,2), E. Simoen (1), K. Opsomer (1,2), D.P. Brunco (1) and M. Meuris (1) 1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium 2. EE Dept., KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium **Resume :** Germanium receives world-wide a renewed interest due to its strong potential as high-mobility channel material for deep submicron high-performance technologies. Ge processing has been demonstrated to be compatible with Si technology and has the important benefit that compared to Si lower thermal budgets are required for dopant activation and implantation-induced defect anneal. However, main challenges remain, like interface passivation, gate stack formation, contact technology, and the fabrication of high-performing n-channel devices. This presentation will review some advanced Ge processing modules from a viewpoint of defect control and engineering. First attention will be given to shallow junction formation, where the thermal anneal procedure must be optimised for minimising the junction depth without compromising the dopant activation and the defect annealing. The discussion will focus on different dopant species such as P, As, B and Sb. Subsequently, the contact technology will be addressed for a variety of germanides, i.e., Co, Cu, Ni, Fe, Pd, Pt, etc. Different structural and electrical analyses, including TEM, DLTS, XRD, and low frequency noise, are combined for determining key aspect such as contact resistivity, defect control and metal diffusion behaviour. The process-induced defects may be caused by implantation damage, metallic contamination in the substrate, and/or sputter damage. The last part will be devoted to integration aspects, pointing out that a control of interaction with point defects and geometrical effects play a crucial role for performance optimization and yield enhancement. add to my program (close full abstract)	91
09:00	B implantation in Ge: electrical and structural investigations Authors : G. Impellizzeri, S. Mirabella, E. Bruno, A. M. Piro, M. G. Grimaldi MATIS CNR-INFM and Dipartimento di Fisica e Astronomia, Universita\\\' di Catania, Via S. Sofia 64, 95123 Catania, ITALY **Resume :** Ge is attracting a renewed interest among scientific community as future material for microelectronics, due to its intrinsic high carrier mobility. Nevertheless, a significant lack of accurate data on dopant diffusion and activation exists. The advantages of B-junctions realized in Ge with respect to Si are the higher hole mobility and the lower B diffusivity, that allows easier dopant confinement. Since the interplay between the excess of point defects, produced during dopant implantation, and the dopant itself is not known, B activation mechanism has to be definitively understood. Dopant implantation creates non-equilibrium conditions in the lattice, heavily affecting the B solid solubility, whose determination span over almost two orders of magnitude in literature. We report a systematic study on B electrical activation. By using four-point probe and Hall techniques (to measure sheet resistance, active dose and carrier mobility) and nuclear reaction analysis (to determine the B total amount and its lattice location), we determined, for the first time, the Hall factor (by which drift- dose and mobility can be derived) at very high dopant densities. Moreover, we studied B behaviour in crystalline Ge and in pre-amorphized Ge and Si, evidencing the advantages of Ge with respect to Si, as the B solid solubility value that is about three times higher in Ge than in Si (the highest value never found). Finally, the thermal stability of such B electrical activation is also reported. add to my program (close full abstract)	92
09:15	Doping of Germanium by Phosphorus Implantation : Prediction of Diffused Profiles with Simulation Authors : S. Koffel P. Scheiblin V. Mazzocchi Cea-Leti A. Claverie Cemes-CNRS **Resume :** The quantitative prediction of doping profiles is mandatory for the elaboration of nanoelectronic devices. Phophorus-doped Germanium is a possible choice for making extensions of advanced p-MOSFETs. In this study, we show that we are able to predict diffusion of implanted Phosphorus in Germanium over the experimental range of interest for MOS application. Wafers made of Germanium epitaxied on Silicon were implanted at various doses and energies and were then annealed with temperatures ranging from 515 to 600 degree Celsius and process times ranging from 10 seconds to 60 seconds. The corresponding SIMS profiles were used as targets for the optimization of the diffusion parameters. Although diffusion in Germanium is often believed to be mediated by vacancies, physical considerations on the damaging of the substrate led us to consider an interstitial-mediated diffusion mechanism. The amorphization caused by the implantation was taken into account to set the initial distribution of point defects. Our predictions of the diffused Phosphorus profiles were obtained using a pair-model with various charge states including solubility limit and outdiffusion. This modelling allowed us to accurately fit with the same set of parameters more than fifteen experimental profiles, even the box-shaped ones that occur at higher thermal budget. add to my program (close full abstract)	93
09:30	Shallow boron implantations in Ge and the role of the pre-amorphization depth	

Authors : E. Simoen1, G. Brouwers1, A. Satta1, M.-L. David2, F. Pailloux2, B. Parmentier1, T. Clarysse1, J. Goossens1, W. Vandervorst1,3, M. Meuris1 1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium 2. Laboratoire de M?llurgie Physique, UMR 6630, Universit?e Poitiers/CNRS, Bd Marie et Pierre Curie, 86962 Futuroscope-Chasseneuil, France 3 IKS-Dept Physics, KU Leuven,Celsetijnenlaan 200-D, B-3001 Leuven, Belgium

Resume : Shallow B implantations are required for the fabrication of the extension junctions in deep submicron CMOS transistors, with a typical depth in the range 10-20 nm. It is well-known that this is a challenge in silicon, due to the Transient Enhanced Diffusion (TED) phenomenon, which originates from the excess ion-implantation induced self-interstitials at the end of range (EOR) damage region [1]. Also for the development of sub-22 nm pMOSFETs on Ge substrates this can be a potential problem, since it is now established that the diffusion of B in Ge is interstitial mediated as well [2]-[3]. The high formation energy of interstitials may explain the low equilibrium diffusivity. Recently, some evidence has been reported about TED of B in Ge, for an implantation energy of 1 keV, which is of interest for extension formation [4]. It is the aim of the present investigation to further study the role of the Ge Pre-Amorphization Implantation (PAI) energy and dose, necessary to suppress the channeling of B ions during subsequent implantation [5]. N-type Czochralski-grown Ge wafers with a diameter of 100 mm have been pre-amorphized by 20, 30, 50 or 80 keV Ge ions with a dose which varied in the range 5x1014 to 1015 at/cm2. Next, B implantations were carried out with energy 1 or 3 keV and doses between 2x1014 and 1015 at/cm2. Dopant activation was performed at 500 oC for 1 min under a nitrogen atmosphere. Chemical profiles in the as-implanted and annealed samples were analyzed by Secondary Ion Mass Spectrometry (SIMS). Carrier profiles and sheet resistances were obtained from Spreading Resistance Probe (SRP) and Variable Probe Spacing (VPS) measurements. The depth of the amorphous-crystalline (a/c) interface was measured by cross-sectional Transmission Electron Microscopy (TEM) – as a rule of thumb, one can state that 1 keV of Ge stands for an amorphization depth of 1 nm in Ge. It will be shown that TED is observed when the a/c interface is in the proximity of the EOR of the B implantation. When the PAI defects are further away, no enhanced diffusion is observed for a 1 minute anneal. Currently, longer anneals are being undertaken to determine whether TED occurs when the a/c interface is further from the depth range of 1 kev B implantation. These observations imply that also for extensions in Ge, point-defect engineering is required to control the junction depth. [1] S.C. Jain, W. Schoenmaker, R. Lindsay, P.A. Stolk, S. Decoutere, M. Willander and H.E. Maes, J. Appl. Phys. 91 (2002) 8919. [2] S. Uppal, A.F.W. Willoughby, J.M. Bonar, N.E.B. Cowern, T. Grasby, R.J.H. Morris and M.G. Dowsett, J. Appl. Phys. 96 (2004) 1376. [3] H. Bracht and S. Brotzmann, Mater. Sci. Semicond. Process 9 (2006) 471. 94

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09:45 Diffusion and activation of Phosphorus in Germanium

Authors : P. Tsouroutas1, D. Tsoukalas1,2 , A. Florakis1, I. Zergioti1, N.Cherkashin2, A. Claverie2, 1 Department of Applied Physics, School of Applied Sciences, National Technical University of Athens, 15780 Zographou, Greece (e-mail: pantsr@central.ntua.gr) 2 CEMES/CNRS, 29 rue J. Marvig, 31055 Toulouse cedex 4, France

Resume : Due to the increased interest of germanium for next generation nanoelectronic devices dopant diffusion studies are critically important. In this work we investigate the diffusion and activation behavior of implanted P in Ge. We use both conventional thermal processing as well as laser annealing by pulsed ns Nd-YAG laser. Chemical and electrical dopant profiles were obtained by SIMS and SRP respectively. Sheet resistance was estimated by Van der Pauw method and the mobility of the carriers was calculated by Hall measurements. These measurements demonstrated a box-shaped dopant profile for both conventional and laser annealed samples which are in agreement with other research reports indicating enhanced dopant diffusivity. >From these experiments and critical comparison with other studies we conclude about the value of the intrinsic diffusion coefficient of phosphorus and we discuss the validity of the double negatively charge vacancy model in simulating our experiments. To more accurately account for these parameters we have also implemented a pile-up and segregation model to simulate the dopant loss due to outdiffusion of phosphorus during the annealing process. In order to understand the influence of defects on transient dopant diffusion as well as on outdiffusion we have also annealed P implanted germanium prior to conventional annealing with laser above melting threshold to eliminate ion implantation defects as these are monitored by Transmission Electron Microscopy. 95

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10:00 Thermal dissolution kinetic of End Of Range Defects in self-amorphized Germanium: an in-situ High Resolution X-Ray Diffraction study

Authors : G. Bisognin 1,2*, S. Vangelista 2 and E. Bruno 3 1 CNR-INFM MATIS, Via Marzolo 8, I-35131 Padova, ITALY 2 Dipartimento di Fisica, Università di Padova, Via Marzolo 8, I-35131 Padova, ITALY 3 CNR-INFM MATIS, Via S. Sofia 64, I-95123 Catania, ITALY

Resume : Ge preamorphization followed by dopants implantation and annealing is a very promising tool to obtain ultra-shallow and electrically active junctions. As in the case of Si(1, a deep understanding both of End-of-Range defects (EORds) and of their dissolution kinetic is a key parameter to get this goal, even if it is still a debated matter. By means of High Resolution X-Ray Diffraction (HRXRD) we measured the perpendicular strain in Ge amorphized with 300 keV, 2.5x10^15 Ge/cm^2 at the liquid nitrogen temperature, detecting a maximum value of 10^-3 just beyond the amorphous/crystal interface. Both the strain position and its sign, which is indicative of interstitial-type defects, are the fingerprint of EORds(1. By performing in-situ HRXRD during isochronal and isothermal annealings in N2 ambient, we monitored the strain (i.e. EORds) till it disappeared (after several hours at 320 °C), finding four dissolution stages. The main stages (I and II), causing the original strain lowering of 50% and 20%, respectively, are characterized by activation energies Ei of EI=1.51 and EII=2.07 eV. The other stages, completing EORds dissolution, have Ei similar to that of Ge solid phase epitaxy (2.2 eV). These data, that will be compared with literature, strongly indicate the presence of four different types of EORds in Ge, also providing an experimental background for EOR atomic structure theoretical investigations. (1 F. Cristiano et al., NIMB, 253, 68 (2006) and refs. therein 96

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(close full abstract)

10:15 n+ doping of Ge by P or As implantation and flash-lamp annealing

Authors : C. Wündisch, M. Posselt, W. Anwand, B. Schmidt, R. Grötzschel, A. Mücklich, W. Skorupa

Forschungszentrum Dresden-Rossendorf, Institute of Ion Beam Physics and Materials Research,
P.O.Box 510119, D-01314 Dresden, Germany E. Simoen, T. Clarysse, A. Satta IMEC, Kapeldreef 75,
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A. Möller, P. Pelzing SGS Institut Fresenius GmbH, Zur Wetterwarte 10, D-01109 Dresden,
Germany
Resume : The increasing interest in Ge as a high mobility substrate has led to numerous
investigations on shallow junction formation by ion beam processing. It has been shown that p+
doping yields junctions with the required properties whereas the formation of n+ junctions is
complicated by the high diffusivity and the low solubility of the dopants. The present work is
focused on the application of flash-lamp annealing to the formation of shallow n+ layers since this 9
method has the potential of good dopant activation while dopant diffusion is suppressed. Shallow 7
layers with high concentrations of P or As are formed by ion implantation. Then the samples are
pre-heated at relatively low temperatures (e.g. 400 °C, for 240 s) in order to achieve the regrowth
of the amorphous layer formed during implantation. Subsequently, flash-lamp annealing is
performed at 800 and 900 °C, for 0.84, 3 and 20 ms. RBS/C is applied to monitor the regrowth of
the amorphous layer. Selected samples are studied by XTEM in order to search for precipitates and
end-of-range defects. The depth distributions of P and As are measured by SIMS. The sheet
resistance of the shallow n+ layer is obtained by the variable probe spacing method. Spreading
resistance profiling is applied to determine the carrier depth profile. Results on phosphorus show
that dopant diffusion only occurs at 900 °C for 20 ms whereas the maximum activation is in the
order of 4-6x1019 cm-3.

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(close full abstract)

10:30 Coffee Break

Joint Session with Symposium J on GeOI and Strain : Cor Claeys, IMEC

11:00 Germanium-On-Insulator MOS Transistor Integration:Challenges and Opportunities for Advanced Technologies

Authors : C. Le Royer, M. Vinet, A. Pouydebasque, C. Tabone, K. Romanjek, P. Batude, L. Hutin, S. Koffel, B. Vincent, F. Mayer, F. Némouchi, E. Augendre, L. Sanchez, H. Grampeix, V. Mazzocchi, V. Carron, P. Scheiblin, J.-F. Damlencourt, J.-M. Hartmann, T. Billon, L. Clavelier and S. Deleonibus : CEA-LETI Minatec

Resume : CEA-LETI is a major actor in the field of Germanium with breakthrough innovations on
both substrates (200mm Germanium-On-Insulator) and MOSFET devices. Large hole mobility
values have been demonstrated in LETI for the two existing approaches for fabricating GeOI: the
Smart Cut process, and the so called "Ge condensation" technique. We have developped a full Si
CMOS compatible process flow to fabricate GeOI MOSFETs. This imply to adapt some specific steps 10
to Ge : resist stripping, gate stack deposition; activation annealing; germanidation… We have 1
reported continuous innovative results for GeOI MOSFETs: the first GeOI pMOSFET in 2005 and
GeOI nMOSFET (on Smart Cut wafers) in 2006; p & nMOSFETs on GeOI obtained by the Ge
condensation technique in 2007. Recently we have corrected the residual p type doping in the Ge
layer leading to controlled threshold voltages. With pockets, we demonstrate the first functional
sub100nm gate length GeOI pMOSFET with excellent ON curents. But in spite of our efforts, the ON
performances of GeOI nMOS are below those of Ge pMOS and Si nMOS. Thus we propose two
possible integration approaches based on the excellent e- and h+ transport properties in Ge and Si
respectively: The planar co-integration of SOI nMOS and GeOI pMOS by local "Ge condensation";
the 3D approach with two different stacked layers sequentially processed: SOI nMOS then Ge pMOS
(thanks to Ge layer transfer after SOI nMOS process, and low thermal budget of Ge MOS process).

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(close full abstract)

11:30 Channel Engineering in MOSFETs

Authors : S.S. Mahato1*, T. K. Maiti1, P. Chakraborty1, S. K. Sarkar2 and C. K. Maiti1 1Department of Electronics & ECE, Indian Institute of Technology, Kharagpur 721302, India 2Dept. of Electronics and telecommunication engineering, Jadavpur University, Kolkata-700032, India

Resume : Technology CAD (TCAD) tools have been used to study the influence of both the uniaxial
(process-induced) and biaxial (substrate-induced) strain on nanoscale MOSFETs down to 22 nm
gate length. The strain in the channel region can be optimized by the optimization of the stress
introduced by the individual process step. Process-induced stress has been introduced using SiGe,
SiGeC, and SiC stressors in the source/drain regions. By changing the Ge content, the stress
distribution in the SiGe source/drain has been engineered and it has been possible to vary the 10
compressive stress in the channel from 255 MPa to 1.8 GPa. In this paper, we investigate the effect 2
of combining the substrate- and process-induced strain together in MOSFETs towards performance
enhancement. By combining both the uniaxial (process-induced) and biaxial (substrate-induced)
strain on nanoscale MOSFETs the drive current is found to improve by ~12%, ~14% and ~19% for
substrate-induced, process-induced and combining the substrate- and process-induced strained
MOSFETs, respectively, over the unstrained Si MOSFET. The RF performance of the both the
process-induced and substrate-induced strain-engineered MOSFETs have been found to be very
high (~500 GHz for n-MOSFETs) compared to unstrained Si MOSFET. Scalability of strained-
engineered MOSFETs and SPICE parameter extraction have also been performed by combining
TCAD and BSIM3 model available in ICCAP

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(close full abstract)

11:45

Strain optimization of Ge/Si samples

Authors : M. Sousa, A. Tapponnier, C. Marchiori, C. Rossel, R. Germann, H. Siegwart, D. Caimi, J. Fompeyrine IBM Research GmbH, Zurich Research Laboratory, CH- 8803 Rueschlikon, Switzerland S. Bedell IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA M. Seo Katholieke Universiteit Leuven, B-3001 Heverlee, Belgium 10

Resume : In the quest of finding a new material set for the next generation of FET devices, 3
strained Ge is investigated as potential channel material because of its enhanced carrier mobility as
compared to Si and its good compatibility with III-V semiconductors. In the frame of this work,
several films of comparable thickness (one series of about 20 nm and another one of about 5 nm)
have been grown by molecular beam epitaxy (MBE) in a dedicated Si-Ge chamber of a multicluster
system from DCA, at temperatures ranging from RT to 600°C on Si (001) substrates. The

crystalline quality of the Ge was monitored in real time by reflection high energy electron diffraction (RHEED) during the growth. The samples have then been structurally characterized by in and out of plane x-ray diffractometry (GIXD and XRD), spectroscopic ellipsometry (SE) and transmission electron microscopy (TEM). X-ray diffractometry measurements for 20 nm thick films reveal that a growth temperature between 100°C and 200°C leads to the highest strain (- 0.8%). Ex-situ post anneals have been performed in addition and show that the Ge crystalline film is fully relaxed when annealed at 400°C. Results performed on films thinner than 20 nm are also presented.

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(close full abstract)

12:00 Stress Analysis of Si1-xGex Embedded Source/Drain Junctions

Authors : M. Bargallo Gonzalez1,2, E. Simoen1, Y. Okuno3, G. Eneman1,2,4, A. Hikavyy1, P. Verheyen1, R. Loo1, C. Claeys1,2, V. Machkaoutsan5, P. Tomasini6, S.G. Thomas6, J.P. Lu7 and R. Wise7 INSTITUTIONS : 1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium 2. EE. Dept., KU Leuven, B-3001 Leuven, Belgium 3. Assignee at IMEC from Matsushita 4. Postdoctoral fellow of the Research Foundation-Flanders (FWO) 5. ASM Belgium, Kapeldreef 75, B-3001 Leuven, Belgium 6. ASM America, 3440 East University Dr., Phoenix, AZ 7. Texas Instruments, 13121 TI Blvd, Dallas, TX 75243

Resume : 1. Introduction. A promising device concept for strained channel pMOSFETs [1], is based on creating uniaxial compressive stress in the channel induced by selective epitaxial growth of Si1-xGex in the Source/Drain (S/D) regions. However, a major concern when technology advances is to maintain the channel stress [2] with the device scaling along the ITRS roadmap. This stress leads to a higher low-field mobility and results in a drive current enhancement. The interest of this work is focused on the analysis of the impact of the Ge content, the epitaxial layer thickness and the active-area dimensions in order to assess the epitaxial quality and the stress levels present in Si1-xGex/Si heteroepitaxial device structures, in the regime where no strain-relaxation processes are present. 2. Experimental. The embedded Si1-xGex S/D junctions were fabricated on 300 mm n-type Czochralski silicon wafers. Active area regions were defined by Shallow Trench Isolation (STI) followed by P and As n-well implantations. Before the selective epitaxial deposition a H2 bake was carried out at 750 oC, 800 oC or 850 oC for 2 min. Subsequent SEG of 100 nm or 140nm in situ highly boron-doped Si, Si0.85Ge0.15 or Si0.75Ge0.25 epitaxial layers, was performed using an ASM Epsilon☐ 3200 reactor, reaching B levels up to 5x1019 cm-3 (evaluated by Spreading Resistance Probe). No implantation, nor anneal, was performed after the epitaxial deposition. As a consequence, the electrical junction is located around the epi/substrate interface. Therefore, the depletion width will be mainly located in the lowly-doped region of the junction, which resides in the Si substrate. Another important observation is that no dislocations were detected by Nomarski optical microscopy, showing no evidence of relaxation in the studied samples. 3. Results and Discussion. The stress was evaluated for fully strained Si1-xGex embedded S/D junctions by three different methods. Firstly, based on the standard elasticity theory model for the electrical characteristics of the p-n junction (current-voltage; capacitance-voltage), which allows to quantify the stressinduced bandgap narrowing in the Si depletion region. Secondly, in order to investigate the window size dependence and the stress distribution along the patterns, Raman Spectroscopy Analysis was performed. Finally, the work was complemented with successfully implemented stress simulations using the SYNOPSYS software package. Acknowledgments. The authors want to acknowledge the contribution of Dr. Nobuyuki Naka from the Semiconductor Systems R&D Department of HORIBA Ltd. for his helpful Raman Spectroscopy analysis. References. [1] M.L. Lee, E.A. Fitzgerald, M.T. Bulsara, M.T. Currie and A. Lochtefeld, J. Appl. Phys. 97 (2005) 011101. [2]G. Eneman, P. Verheyen, R. Rooyackers, F. Nouri, L. Washington, R. Schreutelkamp, V. Moroz, L. Smith, A. De Keersgieter, M. Jurczak and K. De Meyer, IEEE Trans. Electron Dev. 53 (2006) 1647. 10 4

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12:15 Study of N and P type dopants activation and dopants behaviour with respect to annealing conditions in Silicon Germanium On Insulator (SGOI)

Authors : J.Bhandari1,3, M.Vinet1, T.Poiroux1, B.Previtali1,Y.Campidelli2, B.Vincent1, L.Hutin1 J.P.Barnes1, S.Deleonibus1, A.M.Ionescu3 1CEA-LETI/Minatec, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France 2STMicroelectronic, 850 rue Jean Monnet, 38926 Crolles Cedex, France 3Ecole Polytechnique Fédérale de Lausanne, Switzerland

Resume : Reduced parasitic resistance around Source and Drain (S/D) is a major issue in improving the performances of scaled down CMOS. In literature, strain induced by SiGe S/D to channel is said to be responsible for enhancing the device performance. Few publications have reported on study of dopants activation and dopant diffusion c-Si0.7Ge0.3. With this aim, we have investigated the mechanism of electrical activation of dopant in thin SGOI (20nm) material obtained by condensation. The samples are doped either with BF2 or As or P and then spike and 15sec long annealing in the temperature range of 850°C–1050° are performed. SOI (20nm) have been used as a reference for selected conditions for n and p type dopants. Four point probes and Secondary Ions Mass Spectroscopy (SIMS) measurement have been used as characterisation techniques. Sheet resistance (Rs) obtained in SGOI for p-type is approximately independent of annealing conditions. In addition, these values are lower than the SOI reference. Result reveals that almost all BF2 atoms remain in SGOI substrate giving rise to low Rs, whereas dopant out diffuses in SOI. In contrast, Rs measured with As and P implanted SGOI samples are higher then SOI regardless of temperature and time. For all the dopants SIMS profiles are correlated to Rs and dopant behaviours with respect to annealing conditions are discussed. It is concluded that interest on SiGe is also due to high dopant activation making it one of best candidates for modern devices 10 5

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12:30 Lunch

Joint Session with Symposium J on Ge MOS Interfaces and Integration Issues : Thanasis Dimoulas, NCSR DEMOKRITOS

14:00

Comprehensive Evaluation of Ge-Si based High Mobility Channels for Future High Performance Low Power pMOSFETs

Authors : P. Majhi*, J. Oh, S. Lee, W. Loh, R. Harris+, S. Datta, W. Tsai,* H. Tseng, and R. Jammy# SEMATECH, Austin Texas, USA; Assignees from * Intel, +AMD, #IBM

Resume : CMOS scaling has clearly become reliant on new materials and / or new device architecture. With high-k/metal gates into production, promising results on scaled junctions,

contacts and continued progress on process induced strain, CMOS scaling in planar and non-planar architectures will continue for a few more generations. However, it is becoming clear that Si (as the channel) may not be able to provide for the high performance combined with low power technologies that would be needed in future. Despite several years of research on high mobility channels (group IV and III-V) there appears to be little comprehensive work attempting to understand the processing-nanostructure-property interrelationship and thereby address intrinsic 111
advantages and/or limitations of these materials. In this presentation, critical challenges associated with Si-Ge based high-mobility channels for PMOSFETs will be addressed. These include a) heterogeneous integration on Si platform (despite lattice mismatch) b) controlled Ioff and short channel properties (despite smaller bandgap) c) formation of stable gate stacks (despite unstable GeOx) and d) low external resistance (despite lower dopant solubility) respectively. Also, the potential of these channels will be discussed based on benchmarking of the performance of several types of devices on these high mobility channels against state-of-art Si devices.

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(close full abstract)

14:30 Effect of annealing temperature on dielectric properties of selectively formed Ge-on-Si capacitor with high-k dielectric

Authors : Ook Sang Yoo(a,b), Jungwoo Oh(c), Kyung Seok Min(b,d), Chang Yong Kang(c), B. H. Lee (c), Kyong Taek Lee(b,e), In-shik han(a), Hyuk-Min Kwon(a), P. Majhi(c),1, H-H Tseng(c), Raj Jammy(c,2) J. S. Wang(a) and Hi-Deok Lee(a,b) (a) Dept. of Electronics Engineering, Chungnam National University, 220 Gung-dong, Yuseong-Gu, Daejeon, 305-764, Republic of Korea Phone: +82-42-821-7702, Fax: +82-42-823-9544, E-mail: hdlee@cnu.ac.kr (b) University of Texas at Austin, USA (c) SEMATECH, 2706 Montopolis Dr., Austin, TX, 78741 USA, (1) Intel assignee, (2) IBM assignee

Resume : Among the various alternate channel materials, Ge has been recently researched because Ge is most compatible with Si CMOS technology. In order to maximize enhancement of both hole and electron mobility dual channel, CMOSFETs have been proposed, e.i. surface channel for NMOS by using S or s-Si layer and buried channel for PMOS by forming selective Ge layer. In 112
this paper, thin Si capping layer was incorporated on Ge layer for increasing interface quality and Ge pMOSCAP were annealed. We demonstrated dielectric properties of Ge pMOSCAP according to post metallization annealing (PMA) temperatures. SP3 shows lower CV hysteresis. EOT decreases as anneal temperature increases. EOT is 1.59nm (SP3), 1.68nm (for SP2) and 1.7nm (for SP1), which is consistent with results of bulk Ge wafer. However gate current is increased at higher anneal temperature due to the lower EOT. TZDB characteristics was characterized. VBD of SP3 is higher than that of another samples and distribution of VBD after annealing is decreased compare to the SP1. High quality epitaxial Ge layer was formed on n-type bulk Si and capped with 5nm Si layer. PMA was performed in N2 furnace at 400 C, 600C for 60s, SP1 for not annealed sample, SP2 for 400C and SP3 for 600C. SILC measurement was characterized. As a result, Ge pMOS capacitor without PMA shows higher increase of SILC but capacitors with PMA exhibit lower increase of SILC. Thus, it can be believed that PMA reduce bulk traps of gate dielectrics.

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(close full abstract)

14:45 Study of Silicon-Germanium interdiffusion from pure Germanium deposited layers. Application to the formation of gradual SiGe ultra-shallow layers

Authors : M. Gavelle, E. M. Bazizi, E. Scheid, F. Cristiano, LAAS-CNRS, University of Toulouse, 7 avenue du Colonel Roche, 31077 Toulouse Cedex 4, France; C. Armand, INSA Toulouse, Département de Génie physique, 135 avenue de Rangueil, 31077 Toulouse cedex 4, France; P. F. Fazzini, O. Marcelot, CEMES-CNRS, University of Toulouse, 29 rue Jeanne Marvig, BP 9434731055, Toulouse Cedex 4, France; Y. Campidelli, A. Halimaoui, STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles cedex, France.

Resume : Ge-based materials are expected to be progressively introduced in the fabrication of advanced microelectronic devices. SiGe layers are already used as Source/Drain regions to induce uniaxial compressive stress in the Si channel, which results in the enhancement of hole mobility in PMOS. In this work, we study an alternative method for the fabrication of shallow SiGe regions, in 113
which a pure Ge layer is deposited on a Si substrate and the Ge in-diffusion is induced by a subsequent anneal. The optimisation of such a technology requires the accurate measurement of the Ge concentration in the full range of Ge composition and the understanding of the Si-Ge interdiffusion occurring during the formation of the SiGe layers. 300 nm-thick pure Ge(:B) layers were grown on Si 200 mm substrates by CVD at 450°C. As-grown samples were capped with SiO2 and then annealed in the 750°C-900°C range for various times. We present a novel SIMS MCs2+ methodology for the accurate measurement of the Ge diffused profiles. Boltzmann-Matano analysis was used to extract the interdiffusion coefficients. Si-Ge interdiffusion is found to be strongly dependent on the Ge concentration. Also, an effect of dislocations near the Ge/Si original interface is suggested by our results. A physical model including the various observed effects is proposed, that gives a very good agreement with experiments. Finally, we show that the effect of the in-situ B doping of the pure Ge layer is to reduce the interdiffusion.

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(close full abstract)

15:00 XPS and IPE analysis of HfO2 band alignment with high mobility semiconductors

Authors : M. Perego , G. Seguini CNR-INFM MDM National Laboratory, Via C. Olivetti 2, 20041 Agrate Brianza (MI), Italy M. Fanciulli CNR-INFM, Laboratorio Nazionale MDM, via C. Olivetti 2, I-20041 Agrate Brianza (Milano), Italy and Dipartimento di Scienza dei Materiali, Università di Milano Bicocca, Milano, Italy

Resume : The replacement of SiO2 with different high dielectric constant (high-k) materials in metal-oxide-semiconductor (MOS) based devices allows the substitution of Si channel with high-mobility substrates, such as Ge and GaAs. HfO2 and Hf-based oxides are the most promising 114
candidates to be used in advanced microelectronic devices. A key issue for the implementation of these materials as gate oxide is the formation of suitable conduction and valence band barrier at the oxide/semiconductor interface. In this work the band alignment at the interface between HfO2 and high mobility semiconductors (Ge, GaAs) is investigated by means of x-ray photoelectron spectroscopy (XPS) and internal photoemission spectroscopy (IPE). The analysis of XPS results indicates that a differential charging phenomenon originates at the HfO2/GaAs heterojunction during XPS measurements; photoelectrons emitted from the bulk GaAs are compensated by electrons supplied from the ground connection of the sample holder, while those originated in the

ultrathin oxide cannot be fully compensated by electrons from the substrate. Surprisingly this phenomenon is not observed in the HfO2/Ge heterojunction. The determination of the valence band offset requires a careful evaluation of differential charging phenomena and consequently a proper recalibration of the energy scale to remove artifact induced by the X-ray bombardment. The accuracy of the recalibration procedure is validated by the comparison with IPE data.

add to my program **(close full abstract)**

15:15 Influence of the pre-treatment on Co-germanide Schottky contacts

Authors : L. Lajaunie1, M.L. David1, F. Pailloux1, E. Simoen2, C. Claeys2, 3, J.F. Barbot1 1. Laboratoire de Métallurgie Physique, UMR 6630, Université de Poitiers/CNRS, Bd Marie et Pierre Curie, 86962 Futuroscope-Chasseneuil, France 2. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium 3. EE Dept., KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

Resume : Because of its high carrier mobility, Ge is considered as an attractive material for future CMOS technologies. One of the key processes is the formation of a self-aligned germanide layer that reduces the source/drain series resistance. The formation of "good" rectifying contacts is still a tricky problem; their electrical characteristics depend on the surface preparation before metal deposition as well. In this paper, the influence of the pre-treatment on the Co-germanide layer is investigated. Before Co-deposition the samples were subjected to a thermal annealing at different temperatures (400 and 700°C) for a constant duration of 60 min in order to evaporate the native germanium oxide. Then 22nm of Co was deposited by electron-beam evaporation at room temperature under high vacuum. The electrical properties of the as-deposited samples (deep level concentration, leakage current, barrier height,…) are strongly different according to the temperature of the pre-treatment. In addition, a post-metal deposition anneal at 700°C showed that the germanide morphology is also strongly influenced by the temperature of the pre-treatment. In particular the sample annealing at 400°C shows a "engraved" surface with dips up to 500nm in depth. Transmission Electron Microscopy and X-ray Diffraction investigations are in progress to understand the evolution of the microstructure during the whole process. Results will be compared with a HF etching pre-treatment.

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16:00 Coffee Break

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PROGRAM VIEW : 2008

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Front-end junction and contact formation in future Silicon/Germanium based devices

26 May 2008	27 May 2008	28 May 2008	**29 May 2008**	30 May 2008

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start at	Subject	Num.
	Atomistic Simulations II : Lourdes Pelaz, University of Valladolid	
08:30	Challenges for ab initio defect modeling Authors : Peter Deák1, Thomas Frauenheim1 and Adam Gali2 1. U. Bremen, Bremen Center for Computational Materials Science, POB 330440, D-28334 Bremen, Germany 2. Budapest University of Technology & Economics, Dept. Atomic Physics, H-1521 Budapest, Hungary **Resume :** Defect engineering, a key factor in the development of semiconductor technology, has relied, in the past decade strongly on theoretical modeling, where the state-of-the-art is presently represented by ab initio supercell calculations using density functional theory (DFT) in one of the standard implementations: local density or generalized gradient approximation (LDA/GGA). The successes of this technique so far, the substantial growth in computer resources, and the availability of standardized program packages are nowadays leading to “whole-sale” applications with increasing model sizes and/or to dynamic simulations. In face of the increasing complexity of the problems raised by today's technology this seems to be inevitable, but a word of caution is due. The errors connected to the approximations in standard DFT supercell calculations should, at least, be taken into account at the evaluation of the result, or, better, be corrected by more sophisticated methods. We will demonstrate this on an experimentally well documented simple defect: the hydrogen interstitial in silicon, which has several established configurations in the lattice, providing an excellent probe to check on calculations. Invoking also a few other examples, we will call attention to the consequences of the LDA/GGA gap error in the defect properties, which might be much more severe than are usually reckoned with.	12 1
add to my program	(close full abstract)	
09:00	Ab initio calculations of phosphorus and arsenic clustering parameters for the improvement of process simulation models. Authors : Beat Sahli, Kilian Vollenweider Integrated Systems Laboratory, ETH Zurich, Zurich, Switzerland Nikolas Zographos, Christoph Zechner, Synopsys Switzerland LLC, Zurich, Switzerland **Resume :** We present the results of extensive ab initio simulations for phosphorus clusters, arsenic clusters and mixed phosphorus/arsenic clusters in silicon. The specific defects and the parameters that are investigated are selected according to the needs of state-of-the-art diffusion and activation models, taking into account the availability of experimental data, the capabilities of current ab initio methods and the requirements for advanced technology development. The calculated binding energies are used to determine a good starting point for the calibration of a new charged cluster model implemented in the process simulator. The defect species V, I, P, PV, PI, As, AsV, AsI and clusters containing up to four dopant atoms and up to one V or I are considered in all relevant charge states. The ab initio results are discussed as well as the challenges arising in the transfer of this information into the process simulation model.	12 2
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09:15	Atomistic modeling of FnVm complexes in pre-amorphized Si Authors : Pedro Lopez, Lourdes Pelaz Dpto. de Electricidad y Electrónica, Universidad de Valladolid. E.T.S.I. Telecomunicación. Campus Miguel Delibes s/n. 47.011 Valladolid, Spain G. Impellizeri, S. Mirabella, F. Priolo MATIS CNR-INFM and Dipartimento di Fisica ed Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, Italy E. Napolitani MATIS CNR-INFM at Dipartimento di Fisica, Università di Padova, Via Marzolo 8, 35131 Padova, Italy **Resume :** The co-implantation of F and B in pre-amorphized Si has been proved to be beneficial for the fabrication of ultra-shallow junctions due to a remarkable reduction of B diffusion.1 This is attributed to the formation of FnVm complexes during regrowth, acting as annihilation centers for Si interstitials (I´s).1,2 Still, further data on these complexes are needed, as size, F/V ratio (i.e. the number of vacancies per F atom), thermal stability, to better model the I annihilation activity. Based on quantitative data on B diffusion reduction in F enriched Si samples, we have developed an atomistic model to analyze the main features of FnVm complexes, estimating their composition. Whereas the resulting F profile in the recrystallized layer can be easily determined by chemical profiling, the vacancy distribution can only be indirectly estimated.2,3 Our results indicate that the efficiency of FnVm complexes on Si I´s annihilation depends not only on the F/V ratio but also on their size. The hypothesis that the number of F atoms in a FnVm complex is restricted to the number of dangling bonds, as proposed by Lopez et al.,4 may also have a direct influence on the Si I´s annihilation efficiency of the complexes. 1G. Impellizzeri, et al., J. Appl. Phys. 99, 103510 (2006). 2S. Boninelli, et al., Appl. Phys. Lett. 89, 171916 (2006). 3N. E. B. Cowern, et al., Appl. Phys. Lett. 86, 101905 (2005). 4G. M. Lopez, V. Fiorentini, Appl. Phys. Lett. 89, 092113 (2006).	12 3
add to my program	(close full abstract)	
09:30	First principles study of boron in amorphous silicon Authors : Ivan Santos,1,2 Wolfgang Windl,1 Lourdes Pelaz,2 Luis Marques2 1Department of Materials Science and Engineering, The Ohio State University, Coilumbus, OH 43210-1178, USA 2Departamento de Electricidad y Electronica, Universidad de Valladolid, E.T.S.I. de	

Telecomunicacion, 47011 Valladolid, Spain
Resume : Future CMOS technology generations require ultrashallow junctions with high dopant activation levels and very sharp doping profiles. According to the ITRS, solid-phase epitaxial regrowth (SPER) of boron-doped amorphous silicon is a candidate to obtain high active B concentrations. Thus, for the fabrication of state-of-the-art electronic devices, preamorphization implants and high dopant implantation fluences are being used. Boron has been extensively studied in crystalline silicon. However, its behavior in amorphous silicon has been studied to a much lesser degree, especially in the area of an understanding on the atomic level. In order to elucidate the behavior of boron in amorphous silicon, we have carried out ab-initio studies of boron in carefully constructed 64 and 216-atom amorphous silicon cells using VASP. This includes the dependence of the formation energy on the structure (we find that especially the local environment has a crucial influence) as well as the question if there is a distinction between substitutional and interstitial boron analogous to crystalline silicon (which we find is the case). We have also examined the diffusion of boron in amorphous silicon and the dependence of the calculated energetics on the Fermi level (amorphous silicon without defects and impurities has a higher band gap than crystalline silicon). Finally, our results will be compared to available experimental results. 12 4

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09:45 Coffee Break

SiGe and Strain Effects : Martin Hytch, CEMES-CNRS

10:15 Irradiation-induced defects in SiGe
Authors : A.Nylandsted Larsen and A. Bro Hansen, Department of Physics and Astronomy, University of Aarhus, Denmark A. Mesli, Institut d'Electronique du Solide et des Systèmes, CNRS/ULP, Strasbourg, France
Resume : Simple defects in semiconductors, of concentrations sufficient for analysis with standard techniques such as space charge methods, are conveniently produced by irradiation with light particles at MeV energies like electrons and protons. Information on the native point defects, the vacancy and the self-interstitial, can be obtained and, through that, fundamental information on the basic properties of the semiconductors. However, such studies also reveal detailed information on more complex defects which are fundamental to the ion-implantation doping process. Examples of defects in this category are the divacancy, boron-interstitial complexes and the group V - vacancy pair. Parameters extracted from these experiments are indispensable input values in semiconductor process simulation tools. For about ten years, since epitaxial SiGe alloy layers of sufficient quality could be grown on Si sub¬stra¬tes, studies of irradiation induced defects in SiGe have been carried out. Com¬pa¬ri¬sons between defects formed in SiGe and those in pure Si and Ge were made, and the effect of composition on defect-level positions in the band gap and on the thermal stability of the defects was in particular investigated. New defects with no counter partners in pure Si and Ge have also been identified and studied. A review of these investigations based on, in particular, deep level transient spectroscopy methods will be given. The emphasis will be on the effect of composition on defect parameters as only few studies have included the effects of strain. 13 1

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(close full abstract)

10:45 Structural and electrical characterisation of ion-implanted strained Si
Authors : L. O'Reilly (1), K.Horan (1), N. S. Bennett (2,3), A. Lankinen (4), P.J. McNally (1), B.J. Sealy (3), N.E.B. Cowern (2), T.O. Tuomi (4) (1) Nanomaterials Processing Laboratory, Research Institute for Networks and Communications Engineering (RINCE), School of Electronic Engineering, Dublin City University, Dublin 9, Ireland (2) School of Electronic, Electrical and Computer Engineering, University of Newcastle, Newcastle upon Tyne, NE1 7RU, UK (3) Advanced Technology Institute, University of Surrey, Guildford, GU2 7XH, UK (4) Micro and Nanosciences, Micronova, Helsinki University of Technology, P.O. Box 3500, FIN-02015 TKK, Finland
Resume : The production of ultra-shallow junctions for the source/drain extension region using low energy ion-implantation will be required for future CMOS devices. Previously, we have performed extensive electrical measurements on Sb and As ultra-shallow junctions in Si with a strain level of 0.7 %. Biaxial tensile strain reduces the sheet resistance (Rs) of highly doped n-type layers created by a low energy (2 keV) As or Sb ion implantation. The effect can be stronger for Sb, when Rs lowering results not only from strain enhanced mobility, but also from an improvement in Sb solubility with strain present. In a comparison between Sb implants in bulk and strained Si, we find that 0.7% strain has more than doubled the amount of electrically active Sb activated using a low thermal budget rapid thermal anneal at 600 – 700 deg C. We now report on a systematic study over a wide Si strain range from 0.4 to 1.2 % strain in order to establish clear strain-related trends. Prior to implantation the quality of the strained layer and SiGe buffer is assessed using UV micro-Raman spectroscopy, synchrotron x-ray topography (SXRT) and high resolution x-ray diffraction (HRXRD). For measurements of strain following implantation, HRXRD is found to be more accurate than micro-Raman due to an additional carrier-concentration induced Si peak shift in the Raman spectra , which obscures small changes in the strain, resulting from the very high doping levels achieved in these samples, ~7x10^20 cm-3. Using x-ray techniques, at Ge concentrations > than 23% we find clear evidence of tilt in the SiGe virtual substrate, which impacts on the quality of the strained Si. Stacking faults have been detected non-destructively in the Si0.7Ge0.3 geometry samples using SXRT in transmission mode. 13 2

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11:00
High strain amount in recessed junctions induced by selectively deposited B-doped SiGe layers
Authors : H. H. Radamson, M. Kolahdouz, R. Ghandi, and M. ?tling School of Information and Communication Technology, KTH (Royal Institute of Technology) Isafjordsg. 22-26, Electrum 229, 16640 Kista, Sweden Phone: 46-8-7904380 Fax: 46-8-7527850 e-mail: rad@kth.se
Resume : Incorporation of B in strained-SiGe layers has attracted attention during the latest years due to its application in high-frequency HBTs and as stressor layers in source/drain (S/D) areas in pMOSFETs. The later application results in an enhancement in carrier mobility because of the induced uniaxial strain in the channel region. In this design, incorporation of high B concentration is a crucial point for reducing S/D parasitic resistances. The presence of B in SiGe has also been reported to increase the thermal stability of the Ni salicide. On the other hand, B compensates the compressive strain in SiGe layers which is a drawback for the demand of having high strain in the S/D regions. Thus the true guideline in this field points out to high Ge contents and high B 13 3

concentrations for transistor structures. The higher incorporation of boron in SiGe compared to Si layer is believed to originate from presence of strain and higher growth rate during SiGe epitaxy. The former should be dominant for highly B-doped SiGe layers with low Ge contents since the strain in the SiGe may be totally-compensated, whereas the growth rate effect must be more obvious for high Ge contents. To separate the effect of growth rate and strain for B incorporation in SiGe layers is not an easy task since any change in Ge or B concent will affect both these parameters at the same time. In this article, high B amount (1?020-1?021 cm-3) in strained-Si1-xGex (x=0.15 to 0.315) layers grown selectively in recessed openings is presented. The main factors behind the dopant incorporation are investigated. The integration issues were oriented towards having high quality strained layers whereas still high amount of boron is implemented.

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11:15 Optimization of ClusterCarbon™ process parameters for strained Si lattice

Authors : Karuppanan Sekar1, Wade A. Krull1, Thomas N Horsky1, Thomas Feudel2, Christian Krüger2, Stefan Flachowsky2, Ina Ostermay2 1SemEquip, Inc., 34 Sullivan Road, North Billerica, Massachusetts 01862, USA. 2AMD Saxony, LLC & Co. KG, Wilschdorfer Landstr 101, D01109 Dresden, GERMANY.

Resume : As devices approach 32nm regime, scaling becomes more challenging and enhancing performance becomes very difficult. New materials are required to overcome fundamental physical limitations imposed by existing materials. Strained Si is a viable option to sustain continual drive current increase not achieved by traditional scaling. Addition of strained-Si to conventional MOSFET devices is also compatible with existing mainstream CMOS process technology. For the NMOS transistor, strain induced by epitaxially grown Si:C is an option but the difficulty comes in the form of lower throughput and non-repeatable process performance. Monomer carbon implant alone does not result in obtaining the appropriate percentage of substitutional carbon and requires an extra Ge pre-amorphization (Ge-PAI) step. With the self-amorphizing capability of ClusterCarbon implant (thus avoiding an extra Ge-PAI step) it has been shown that one can introduce about 2% of substitutional carbon after suitable anneal. Thus Si:C formation by ClusterCarbon implant is more appealing and a promising contender for high performance device applications. In this work we will present the substitutional carbon dependence of ClusterCarbon implant energy & dose, and anneal parameters such as solid phase epitaxial regrowth (SPER) soak time and temperature and various high temperature millisecond anneal conditions. It is been established that optimizing the percentage of [C]sub requires SPER anneal temperature < 850oC followed by a millisecond anneal. Substitutional carbon fraction in implanted samples approaches the ideal 100% limit if the optimized anneal process includes a millisecond anneal process like flash or laser anneal. Stress/Strain and the percentage of substitutional carbon will be discussed from data obtained using UV Raman measurement, high resolution x-ray diffraction (HRXRD) method and SIMS measurements. The amorphous layer thickness by ClusterCarbon implant using XTEM will be correlated to the % of substitutional carbon obtained from HRXRD measurements. Dependence of substitutional carbon percentage on various implant and anneal parameters will be presented and discussed. 134

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11:30 Effects of doping on the elastic properties of silicon

Authors : N. Santen and R. Vianden Helmholtz - Institut für Strahlen- und Kernphysik, 53115 Bonn, Germany

Resume : At present, the use of strained silicon in the design of high performance devices has been shown to be very successful. However, even if the method has found wide application many open questions still persist. A lot of interesting aspects in conjunction with the influence of dopant atoms on the elastic properties of silicon have not yet been fully understood or even studied. The perturbed angular correlation method (PAC) is well suited for studying strain on an atomic scale. Thus, we are able to investigate both externally applied tensile/compressive stress and also local lattice distortions, which arise in implanted regions due to the mismatch of the radii of lattice and dopant atoms. Furthermore, the impact of different dopant atoms on the elastic properties of the silicon lattice is studied using the acceptor 111-In as probe. It was found that the response of the silicon lattice to mechanical stress showed strong differences depending on the dopant species. Current experiments show that doping with donors and acceptors alters the elastic properties of silicon in a different way. 135

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11:45 Local strains induced in silicon by a periodic array investigated by High-Resolution X-Ray Diffraction

Authors : S. Escoubas 1,2, O. Thomas 1,2, F. Cacho3, G. Raymond3, P. Morin3 1 Aix-Marseille Université, IM2NP 2 CNRS, IM2NP (UMR 6242) Faculté des Sciences et Techniques, Campus de Saint-Jérôme, Avenue Escadrille Normandie Niemen, Case 262, F-13397 Marseille Cedex, France 3 ST Microelectronics, 850 rue Jean Monnet, F-38926 Crolles, France

Resume : Stress engineering is becoming of increasing interest to enhance microelectronics device performance in particular by improving electron or hole mobility. For that purpose, one way is to stress the transistor Si channel by depositing a strained layer on top of the polysilicon gate. Silicon nitride is a good candidate as the layer can be either tensile or compressive depending on the process parameters. Even though the strain field induced in silicon can be predicted with the help of finite elements modelling, corroborating the calculated strain field with measurements is crucial. As a consequence, measuring strains or stresses at the nanometer scale is a real challenge. In this study we investigate the periodic strain field in silicon with high resolution X-ray diffraction. X-ray diffraction is very sensitive to local strains (<10-4) and has the distinct advantage of being non destructive. Investigated samples are periodic arrays of polysilicon lines deposited on thermally oxidized single crystal (001) Si substrate and capped with silicon nitride. The periodicity is shrinked down to 200 nm with a line width of 65 nm representative of the devices actually in production. The X-ray measurements have been performed on a 4 circles goniometer with a sealed tube, Ge (220) Bartels primary optics and Ge (220) three bounce analyser. We have recorded both symmetric and asymmetric reciprocal space maps around the Si substrate Bragg peak, in order to extract axial strains in the 3 directions. The strain field periodicity induced in silicon by the capped polysilicon lines gives rise to satellites in reciprocal space. The intensity of these satellites is directly related to the strain field in silicon. Elastic calculations are performed with a Finite Element Modelling code in order to extract the displacement field that is used for structure factor calculations within 136 kinematical approximation. Finite Element Modelling is also compared with analytical modelling, using a line force model. The calculated reciprocal space maps are finally compared with X-Ray Diffraction measurements.

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12:00 Lunch

Basic Diffusion, Activation, and Defect Formation Studies : Peter Pichler, Fraunhofer IISB

13:30 Boron diffusion in crystalline and amorphous silicon.

Authors : Davide De Salvador, Enrico Napolitani, Gabriele Bisognin, Maurizio Pesce, Alberto Carnera MATIS, CNR-INFM and Physics Department, University of Padova, Padova, Italy. Salvo Mirabella, Elena Bruno, Giuliana Impellizzeri, Emanuele Francesco Pecora, Francesco Priolo MATIS, CNR-INFM and Physics and Astronomy Department, University of Catania, Catania, Italy.

Resume : Boron, as the main p-type dopant in Si, has been extensively investigated both experimentally and theoretically in order to understand its diffusion mechanisms for modelling and optimization of advanced devices. Crystalline Si matrix was mostly studied, but quite recently increased interest emerged on the behaviour of B in amorphized Si. In this work we present our recent progress in understanding these fundamental processes. In crystalline phase, thanks to advanced experimental methods, we measured with an unprecedented level of accuracy and sensitivity, the key parameters describing the B diffusion in different equilibrium conditions i.e. in wide ranges of temperature, doping level and doping kind. On this basis, a comprehensive, experimentally based, atomistic model for B diffusion has been assessed, advancing and clarifying in a coherent picture the wide existing literature, including the interactions among B, self-interstitial in different charge states, free carriers and co-doping species (pairing). Also the amorphous phase shows a complex B diffusion mechanism, far from being Fick-like. By means of simulation modelling of extensive diffusion data, produced in a wide range of temperatures, times and B concentrations, we demonstrate that B promotes the formation of dangling bonds and interacts with them in order to diffuse. Peculiar physical features, such as diffusion shape and transient diffusion, are correctly described by the model. 141

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14:00 EVOLUTION OF BORON-INTERSTITIAL CLUSTERS IN PREAMORPHIZED SILICON WITHOUT THE CONTRIBUTION OF END-OF-RANGE DEFECTS

Authors : Maria Aboy, Lourdes Pelaz University of Valladolid, Campus Miguel Delibes, 47011 Valladolid, Spain E. Bruno, S. Mirabella MATIS CNR-INFM Via Santa Sofia 64, I-95123 Catania, Italy E. Napolitani MATIS CNR-INFM at Dipartimento di Fisica, Via F. Marzolo 8, I-35131 Padova, Italy

Resume : Low-energy B implantation into preamorphized Si and subsequent solid phase epitaxial regrowth (SPER) techniques appear to be necessary to achieve proper junction performance in PMOS transistors. After SPER, B concentrations up to a few times 1e20 cm-3 are electrically active whereas higher B concentrations remain inactive, immobilized in boron-interstitial clusters (BICs). During anneal after SPER, end-of-range (EOR) defects present beyond the amorphous/crystalline interface lead to changes in source/drain extensions sheet resistance (RS) and B redistribution. However, there are still some uncertainties about the configurations of BICs that results after SPER and the mechanisms causing variation of RS increase. We have designed a fundamental experiment based on B implanted into preamorphized Si with EOR defects placed far enough from the B profile, in order to avoid the interaction between EOR defects and resulting BICs during annealing after SPER. Kinetic Monte Carlo (KMC) simulations combined with Hall measurements (to extract active B dose, RS and hole mobility) indicates that initial BICs should not contain a high amount of Si interstitials. Otherwise BICs would grow excessively, even without EOR influence, contrary to experiments. At very high B concentrations, it appears necessary to extend BIC models up to larger and more stable configurations than modeled before, as suggested by previous experimental work [1]. [1] F. Cristiano et al., Appl. Phys. Lett. 83, 5407 (2005) 142

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14:15 BORON OUTDIFFUSION MECHANISM IN OXIDE AND NITRIDE CMOS SIDEWALL SPACER: IMPACT OF THE MATERIALS PROPERTIES

Authors : B.Pelletier(a,b), P.Morin(a), D.Beucher(a), M.Juhel(a), JL.Autran(a,b) (a) STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France (b) IM2PN UMR CNRS 6242 & Universités Paul Cézanne, Provence et Sud Toulon Var, France

Resume : The continuous scaling in microelectronics requires a parallel effort in ultra-shallow junction development and modelling. In traditional CMOSFET process flow, sidewall spacer are introduce after the lightly doped drain (LDD) implant, to keep the source/drain doping species away from Si channel, to minimize the hot carrier and the short channel effects. Standard sidewall spacers are made of nitride layer deposited upon thin silicon oxide film which acts as a stop layer during the spacer nitride anisotropic dry etch. In recent technology nodes a huge effort has been done to decrease the thermal budget of the deposition processes, to avoid boron diffusion from the extension into the Si channel. Several studies have shown an interaction between the spacer and the LDD extension. In particular, the hydrogen concentration of the oxide liner enhances the boron out-diffusion from LDD into the oxide resulting in significant dose loss within the junction. We present in this paper a study of the boron out-diffusion mechanism and a comparison of the effects induced by different type of nitride film used in spacer application. Different stacks composed of boron doped Si wafer/oxide/nitride have been submitted to a rapid thermal annealing similar to the activation process used in recent CMOS technologies. The wafers are analysed by SIMS technique to obtain the boron profile within the stack. These profiles allow the extraction of the activation energy and to compare the diffusion mechanism for each type of nitride film. We observe that the magnitude of this diffusion effect on advances technologies is so important that the understanding the mechanism is mandatory for an efficient junction optimisation and modelling. 143

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14:30 Nanoscale Implantation-Induced Mixing and Transient Enhanced Diffusion of Silicon Revealed by Isotope Superlattices

Authors : Yasuo Shimizu[1], Masashi Uematsu[1], Kohei M. Itoh[1], and Akio Takano[2] [1] Department of Applied Physics and Physico-Informatics, Keio University, Yokohama 223-8522, Japan [2] NTT Advanced Technology Corporation, Atsugi 243-0124, Japan

Resume : Si isotope superlattices composed of alternating layers of 92.3% Si-28 (10 nm) and 99.92% Si-28 (10 nm) stable isotopes have been employed to evaluate quantitatively the host Si atomic displacement induced by ion-implantation, condition for amorphization by implantation, and Si self-interstitial diffusion during the transient enhanced diffusion (TED) annealing after implantation. Statistical evaluation of the intermixing probed by SIMS of Si isotopes between adjacent layers as a result of As and Sb implantations allows for the quantitative determination of the Si atomic displacements of the order less than 1 nm as a function of the depth. Combination of the SIMS and TEM reveals that the Si displacement of 0.5 nm is the critical length for the 14
amorphization. TED of Si was observed as the followings. B ions were implanted with the dose of 4
3×10^{14} cm^{-2} and 12 keV into the isotope superlattice followed by 850 ^{o}C TED annealings for 1-4 hours. Si self-diffusion much faster than that of equilibrium diffusivity was then observed within the first 1 hour of annealing, confirming TED of Si. Implementation of these findings is expected to improve the accuracy of the nano-CMOS process simulators significantly. The work has been supported by the Research Program on Collaborative Development of Innovative Seeds by JST, Special Coordination Funds for Promoting Science and Technology, and G-COE program on Leading-Edge Platform on Access Spaces by MEXT.

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14:45 NANO-BUBBLES INDUCED IN AMORPHOUS AND CRYSTALLINE Si BY F-IMPLANTATION

Authors : S. Boninelli1, G. Impellizzeri1, S. Mirabella1, F. Priolo1, E. Napolitani2, N. Cherkashin3, P.F. Fazzini3, and F. Cristiano4 1 MATIS CNR-INFM and Dipartimento di Fisica ed Astronomia, Università di Catania, Via Santa Sofia 64, 95123 Catania, Italy 2 MATIS CNR-INFM and Dipartimento Fisica, Università di Padova, Via F. Marzolo 8, 35131 Padova, Italy 3 CEMES-CNRS, 29, Rue Jeanne Marvig, 31055 Toulouse 4 LAAS-CNRS, 7, Avenue du Colonel Roche, 31055 Toulouse

Resume : The beneficial effects of F implantation on the reduction of B diffusion in Si is generally recognized. However, the physical mechanisms responsible for the observed effects are still under debate. To investigate the structural modifications due to the F introduction, we implanted 6 x 1015 F/cm2 at 75 keV in preamorphized Si. After that, some samples were partially recrystallized by solid 14
phase epitaxy (SPE). Transmission electron microscopy (TEM) images present a band of bubbles 5
(with a diameter of about 3.5nm) in the residual amorphous region, overlapping the highly F enriched region, as shown by secondary ion mass spectrometry analysis. These findings clearly indicate that the formation of F-induced bubbles occurs already in the amorphous phase. Once formed, the F-V clusters remain stable after the complete Si crystallization. The thermal evolution of these bubbles in recrystallized samples has been studied and their density and size distribution has been evaluated. Moreover, in order to study the effect of these F-V complexes on extended defects, we have demonstrated that they act as trapping centers for the Si self-interstitials, preventing the formation of extended defects. These results will have important implications in the development of predictive models for the fabrication of ultra-shallow junctions using point defect engineering.

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15:00 Evolution of end-of-range defects in Silicon-On-Insulator substrates

Authors : P.F. Fazzini(a), F. Cristiano(b), C. Dupré(c,d), S. Paul (e), T. Ernst(c), H. Kheyrandish(f), K.K. Bourdelle(g), W. Lerch(e) a - CEMES/CNRS, University of Toulouse, 29 Rue Jeanne Marvig, 31055 Toulouse Cedex 4, France b - LAAS/CNRS, University of Toulouse, 7 Avenue du Colonel Roche, 31077 Toulouse Cedex 4, France c - CEA-LETI, Minatec 17 Avenue des Martyrs, 38054 Grenoble Cedex 9, France d - IMEP Minatec- 3 parvis Louis Néel, 38 016 Grenoble Cedex 1, France. e - Mattson Thermal Products GmbH, Daimlerstr. 10, D-89160 Dornstadt, Germany f - CSMA-MATS, Stoke-on-Trent, Staffordshire , ST4 7LQ, UK g - SOITEC, Parc Technologique des Fontaines, Bernin 38926, Crolles Cedex, France

Resume : The use of Silicon-On-Insulator (SOI) substrates provides significant advantages for the fabrication of the next-generation of electronic devices. Improved speed and reduced power consumption in CMOS devices are just some of the important improvements resulting from the insulating properties of the buried SiO2 layer (BOX). Conversely, the effects of the BOX on the 14
evolution of the End-of-Range (EOR) defects are not very well understood. However, the detailed 6
knowledge of these phenomena is mandatory to accurately control dopant diffusion and activation in the SOI substrates. In this work we study the evolution of the EOR defects, in germanium-implanted SOI wafers of variable thickness and in bulk silicon wafers. The amorphizing implants creating the EOR defects were followed by a series of anneals. TEM and SIMS analyses have been performed to obtain detailed information on defect evolution. A considerable reduction of the EOR defect density has been observed in the SOI wafers as compared to the bulk Si wafers. We observe that the total defect density is reduced as the Si over-layer thickness decreases. For the SOI substrates the EOR density reduction is not related to the implant dose loss in the BOX but is rather associated with the effects of the top Si/BOX interface . The results have been interpreted using an advanced defect simulation model in which the top Si/Box interface acts has an effective sink for interstitials diffusing out of the EOR defect region.

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15:15 The use of extended-defect dissolution as a probe for stress-induced interstitial diffusion anisotropy

Authors : P. Castrillo (1), R. Pinacho (1), M. Jaraiz (1), J. E. Rubio (1) and J. Singer (2) (1) Dept. Electronics, University of Valladolid, 47011 Valladolid, Spain (2) NXP Semiconductors, 38926 Crolles, France

Resume : Strained silicon is essential for 45-nm node and beyond in order to improve carrier mobility. This strain could induce defect and dopant diffusion anisotropy during device processing. At the present there is a controversy in the theoretical studies about the magnitude of this 14
anisotropy. Besides, available experimental measurements on diffusion anisotropy in Si are indirect 7
and only concerning dopants. In this paper we analyze the effect of interstitial diffusion anisotropy on extended defect dissolution and we propose an experimental method to estimate it. We have implemented the effects of biaxial stress in the atomistic KMC simulator DADOS. Possible defect diffusion anisotropy has been included through the perpendicular and parallel components of the migration strain tensor (Vm_perp and Vm_paral). The possible strain-dependence of binding energies of extended defects has been also included. We have simulated damage evolution induced by Si-implant during subsequent annealing in biaxially strained silicon, with Vm_perp and Vm_paral

values varying within the plausible ranges. Significant changes in the competition between {311}-defect dissolution and ripening have been observed. We show that the plot of {311} density versus {311} mean size is a fingerprint of interstitial diffusion anisotropy and suggest a method to experimentally determine its presence and value.

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15:30 Coffee Break

Advanced Device Concepts and Simulation : Jean-Michel Hartmann, CEA-LETI

16:00 Optimization of Si:C Source and Drain Formed by Post-Epi Implant and Activation Anneal: Experimental and Theoretical Analysis of Dopant Diffusion and C Evolution

Authors : Y. Cho(1), N. Zographos(2), S. Thirupapuliyur(1), V. Moroz(3), L. Date(1), R. Schreutelkamp(1), Y. Kim(1), Z. Ye(1), S. Chopra(1); 1 - Applied Materials, Inc.; 2 - Synopsys Switzerland LLC; 3 - Synopsys, Inc

Resume : The nFET device performance improvement has been demonstrated using recessed source and drain (S/D) Si:C approach and considered for added strain solution for nFET performance for 32nm technology and beyond. Obtaining and retaining high Csub and proper junction formation are critical in fully realizing device performance benefit. Junction formation by both in-situ doping and post-epi implant and activation anneal of undoped Si:C epi have been investigated. In this paper, experimental P and As dopant diffusion in Si:C epi films containing >1% C is presented. A modified diffusion model was developed for dopant implanted SiC epi films by incorporating special effects (e.g. C-rich clusters and unusual vacancy super-saturation) not captured in previous models developed for C and dopant co-implant case. Epi layer structure evolution is analyzed based on physical film characterization by high-resolution x-ray diffraction technique. Multi-layer analysis was utilized to characterize non-uniform Csub profile in the film and explain the film evolution through the doping sequence. Experimentally and theoretically, Csub profile and retention in Si:C epi are analyzed as a function of dopant implant energy and activation (spike) anneal temperature. For improved Csub retention, use of advanced millisecond (ms) laser anneal was investigated. Near 100% Csub retention with no compromise in junction depth is observed when P implanted Si:C epi film is activated by ms laser anneal. 151

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16:30 Novel Enhanced Stressors with graded encapsulated SiGe embedded in the source and drain areas

Authors : Andreas Naumann*, Stephan Kronholz , Anthony Mowry#, Ina Ostermay*, Helmut Bierstedt , Bernhard Trui , Kornelia Dittmar , Thorsten Kammler *Fraunhofer-Center Nanoelectronic Technologies, Königsbrücker Landstr.180, 01099 Dresden, Germany AMD Saxony LLC & Co.KG, Wilschdorfer Landstr.101, 01109 Dresden, Germany # Advanced Micro Devices, 5204 East Ben White Blvd., Austin TX 78741, USA

Resume : An advanced CMOS scheme for the integration of a graded epitaxial Silicon Germanium (SiGe) layer is presented. SiGe is deposited into the source drain regions right after gate formation. The SiGe layer is exposed to process steps such as cleaning, implantation and annealing which cause erosion, dopant loss and crystal defects. This effect is aggregated with increasing Ge content, while higher Ge content is wanted to increase stress in the channel and thus improve charge carrier mobility. The negative effect of SiGe erosion on DC transistor performance is shown in this paper and how it can be reduced by optimized SiGe deposition utilizing a two layer stack with different Ge percent. First a film with higher Ge concentration is deposited followed by a low percent Ge film. The top layer with the lower percent Ge is aimed to be a protection for the underlaying higher Ge stack. Electrical data for PMOS devices with 550?embedded SiGe with 20-30% Ge are presented and compared with the corresponding graded SiGe stack (25-30%, 500?with 50?thick 15% cap). Comparing a 30% SiGe film with the graded version we see an improvement of 5% for IDSAT. The experiment is executed both on a LPCVD reactor as well as on an UHV-CVD system resulting in matched deliverables, demonstrating that the erosion is independent from deposition but caused by material properties. TEM pictures confirm that the SiGe erosion is fairly reduced by using the graded layer stack. 152

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16:45 Gate-Length Scaling Trends of Drive Current Enhancement in CMOSFETs with Dual Stress Overlayers and Embedded-SiGe

Authors : S. Flachowsky (a), A. Wei (b), T. Herrmann (a), R. Illgen (a), M. Horstmann (b), R. Richter (b), H. Salz (b), W. Klix (a), and R. Stenzel (a) (a) Department of Electrical Engineering, University of Applied Sciences Dresden, Friedrich-List-Platz 1, 01069 Dresden, Germany, stefan.flachowsky@et.htw-dresden.de, (b) AMD Saxony LLC & Co. KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Germany

Resume : A comprehensive study of strain engineering in MOSFETs using tensile nitride overlayer films (TOL), compressive nitride overlayer films (COL), and embedded-SiGe (eSiGe) is studied by extensive device experiments and numerical simulations. The scaling behavior was analyzed by gate length reduction down to 40nm and it was found that drive current gain increases first with decreasing gate lengths, saturates for mid-length devices at around 70nm, and actually decreases with further reduction in gate length. This rolloff effect was studied and well reproduced by 2D process and device simulations. It can be attributed to two competing factors: shorter gate-length devices have increased longitudinal and vertical stress components which should result in improved current gains. However, there is a larger degradation from external resistance as the gate-length decreases, due to a larger voltage dropped across the external resistance. Thus, these parasitic resistances mask the tensile and compressive overlayer benefit for devices with gate lengths shorter than ~70nm. In the linear current regime, this rolloff shifts to shorter gate lengths due to the reduced effect of external resistance at lower voltage. Adding an eSiGe stressor also reduces the external resistance in the p-MOSFET, to the extent that that the current gain from COL continues to increase even down the the shortest gate length studied. This is due to the reduced resistivity of SiGe itself, and the smaller contact resistance from a barrier height reduction (smaller SiGe bandgap). This shows the advantage of combining eSiGe and COL, not only for increased stress and higher boron solubility, but also for parasitic resistance reduction to enable better COL drive current benefit. 153

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17:00 Simulation of the deactivation of arsenic during thermal processes after activation by SPER

Authors : A. Martinez-Limia, P. Pichler Fraunhofer Institute of Integrated Systems and Device Technology, Schottkystrasse 10, 91058 Erlangen, Germany W. Lerch, S. Paul Mattson Thermal Products GmbH, Daimlerstrasse 10, 89160 Dornstadt, Germany H. Kheyrandish CSMA – MATS, Queens Road, Stoke on Trent ST4 7LQ, United Kingdom A. Pakfar, C. Tavernier STMicroelectronics SA, 850 rue Jean Monnet, 38926 Crolles, France

Resume : With decreasing device dimensions, new challenges arise for process developers. Shallow, highly doped junctions are required to meet the requirements of the industry in the near and mid-term future. While implantation processes go to higher doses and lower energies, some replacement will also be needed for the currently used spike annealing technology. One actively pursued annealing strategy which is considered a viable alternative for future technology nodes is based on low-temperature thermal processing after amorphizing implantation to take advantage of the high activation of dopants after solid phase epitaxial regrowth (SPER). The goal is to achieve active dopant concentrations around and, if possible, above the solubility limit in silicon. Especially critical is not only the state after SPER but also the deactivation after SPER during subsequent annealing steps required during the further processing of the device. In this contribution we present a detailed study of the deactivation of arsenic after activation by spike annealing or low-temperature SPER. The experimental results are also compared to simulations of the respective processes using a previously developed calibrated model for arsenic diffusion and deactivation. The specific contributions to deactivation via different processes like clustering, precipitation, and segregation is discussed and annealing strategies to minimize the deactivation are proposed. 154

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17:15 SIMULATION OF THE SUB-MELT LASER ANNEAL PROCESS IN 45 CMOS TECHNOLOGY – APPLICATION TO THE THERMAL PATTERN EFFECTS

Authors : A. Colin (a,b), P. Morin (a), F. Cacho (a), H. Bono (c), R. Beneyton (a), M. Bidaud (a), D. Mathiot (b), E. Fogarassy (b) (a) STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France (b) InESS (CNRS and Université Louis Pasteur), BP 20 CR, 23 rue de Loess, 67037 Strasbourg Cedex 2, France (c) LETI, CEA-Grenoble, 17 Rue des Martyrs, 38054 Grenoble Cedex 9, France

Resume : Due to the continuous CMOS transistor scaling requirements, highly doped ultra shallow junctions with improved activation are deeply investigated. In this scope, sub-melt millisecond laser annealing has been introduced in 45 nm CMOS technology to enhance dopant activation without any additional diffusion detrimental to the device. At the step of the activation anneal, the transistors are composed of different stacks of silicon (junctions), polysilicon (gate), silicon oxide (shallow trench isolation) and/or silicon nitride films which present sensitive differences in optical and thermal properties. Because of the design, the active and the gate layout introduces significant variations of densities and geometries that can induce temperature non uniformities over the die, often called “pattern effects”. The introduction of an absorbent layer above the wafer reduces the optical variations, but the temperature variations generated by the thermal properties non homogeneities can't be suppressed. The impossibility to measure directly this transient temperature effects on a device requires simulation. In this paper, we present a thermal simulation developed to model with accuracy the laser annealing with the real process parameters which was validated by pyrometer and sheet resistance measurements. This model is used to obtain the transient temperature distribution over the devices, which is needed to understand the laser impact on the transistors performance. In addition, it allows studying the thermal pattern effects. Depending of the layout density of shallow trench isolation, temperature variations up to 50°C over a die can be observed. Finally, the simulation can provide guidelines for minimising pattern effects. 155

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17:30 The impact of nitrogen co-implantation on boron ultra-shallow junction formation and underlying physical understanding

Authors : S. H. Yeong #/*, B. Colombeau *, K. R. C. Mok *, F. Benistant *, C.J. Liu ^, A. T. S. Wee ^, L. Chan * and M. P. Srinivasan# #Department of Chemical and Biomolecular Engineering, National University of Singapore, 9 Engineering Drive 1, Singapore 117576 *Chartered Semiconductor Manufacturing Ltd, 60 Woodlands Industrial Park D, Street 2, Singapore 738406 ^Department of Physics, National University of Singapore, 9 Engineering Drive 1, Singapore 117542

Resume : Ultra-shallow junction (USJ) formation is one of the immense challenges in the sub-45nm CMOS technology node. Co-implantation of fluorine (F) and carbon (C) in boron (B) doped preamorphized silicon has been shown to reduce B transient enhanced diffusion (TED) and suppress dopant deactivation. However, nitrogen (N) co-implantation for USJ is less established. In this work, we present an extensive study on the impact of N co-implant in preamorphized B USJ. All wafers were implanted with 15keV Ge and followed by 1keV B and some were co-implanted with 2keV, 6keV or 25keV N. Our results show the B TED can be reduced to different extents by varying the distribution of N atoms. This is attributed to the relative location of N with respect to the B profile and end-of-range (EOR) defect band, affecting the interactions between the dopants and defects during the annealing. In addition, significant variations in B dopant activation and deactivation are also observed. Similar to the F atoms, it is proposed that for PAI case N react with vacancy point defects to form NV complexes that will trap the interstitials emitted from the EOR region. However, the study clearly demonstrates that the interstitial trapping of N is not as efficient as C. We also reveal that EOR defects can be stabilized by choosing the optimized N co-implant condition. Based on our study, a physical modeling on the diffusion/clustering pathways of N is shown to explain the B diffusion and deactivation behaviors. 156

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