Strasbourg (France)

E-MRS 2005 Spring Meeting

May 31 – June 3, 2005

SYMPOSIUM D

Materials science and device issues for future Si-based technologies

Symposium Organizers :

Fuccio Cristiano, LAAS/CNRS, Toulouse, France

Benjamin Colombeau, Charactered Semiconductor Manufacturing, Singapore

Ray Duffy, Philips Research, Leuven, Belgium

Lourdes Pelaz, University of Valladolid, Spain

Suresh Uppal, University of Southampton, U.K.

Symposium Support :

Papers to be published in
Materials Science and Engineering B

E-MRS 2005 Spring Meeting

SYMPOSIUM D

Tuesday, May 31, 2005 **Morning**
Mardi 31 mai 2005 Matin

Session I : Advanced devices
Session chair: E.A. Fitzgerald

9:00 **OPENING**

D-I.01 9:10 -Invited-

NEW MATERIALS AND DEVICE ARCHITECTURES FOR THE END-OF-ROADMAP CMOS NODES

Thomas Skotnicki, ST Microelectronics, Crolles, France

D-I.02 9:40 -Invited-

AB-INITIO ASSISTED PROCESS MODELING FOR Si-BASED NANOELECTRONIC DEVICES

Wolfgang Windl, Dept. of Materials Science and Engineering, The Ohio State University, Columbus OH, USA

The continuing miniaturization of semiconductor devices has currently reached a stage where further progress does not seem to be feasible for much longer. Several dimensions are about to meet their physical limits (like the thickness of the gate oxide or dopant concentration vs. junction depth in ultrashallow junctions) and require novel solutions. Even where traditional device recipes can still be used, the presence of only a "few" dopant atoms questions more and more the use of mean-field theories and at the same time makes previously spurious effects important like dopant dose loss at interfaces. This situation requires stronger attention to the single atoms and their role in the device.
In this talk, we will examine the role of atomistic simulations - mostly on the basis of quantum mechanical ab-initio methods - for current and future process simulation. This will range from "atomistic enhancements" of traditional process modeling to include small-scale effects such as dose loss or segregation to completely atomistic process modeling based on MD and kinetic lattice Monte Carlo techniques. In a further step, we will discuss simultaneous process and device modeling on the atomic scale for the example of carbon nanotube Schottky devices. Finally, we will discuss the nanoscale characterization problem, where traditional techniques such as SIMS or traditional TEM work do not give the needed information anymore. We will present coupled experimental-theoretical methods that can detect single dopant atoms and even allow to "see" the atomic structure of amorphous oxide layers.

D-I.03 10:10

INFLUENCE OF THE SPACER DIELECTRIC PROCESSES ON PMOS JUNCTION PROPERTIES

P. Morin, F. Wacquant, M. Juhel, D. Lenoble, C. Laviron, ST Microelectronics, 850 Rue Jean Monnet, 38926 Crolles, France

In a standard CMOS integration flow, spacer silicon oxide and nitride films are deposited after Lithely Doped Drain implantations. Final spacers are then completed by an anisotropic dry etching process. While shallow junctions are required to minimize short channel effects, final junction depth can be significantly increased by diffusion occurring during the spacer dielectrics deposition processes, due to their thermal budgets. Despite the introduction of low thermal budget oxide and nitride, significant diffusion phenomena are still visible, especially on pMOS junctions. Recent works have described a boron dose loss phenomena occurring during the final activation anneal, enhanced by the oxide hydrogen concentration.
In this paper, we compare different standard and low thermal budgets oxide and nitride spacer dielectrics. Different trials on both full flow and full sheet wafers have been carried out. On these wafers, boron profiles were evaluated by Secondary Ion Mass Spectroscopy. These experiments confirm the H mechanism already described in literature and show the influence of the nitride porosity on the boron out diffusion. In addition, we study in detail the influence of the deposition process thermal budgets on hydrogen content and boron dose loss.

D-I.04 10:25

NOVEL APPROACHES TO IMPROVE LASER ANNEALED SOI-MOSFETS

T. Herrmann(a), Th. Feudel(b), M. Horstmann(b), J. Hoentschel(b), L. Hermann(b), W. Klix(a) and R. Stenzel(a), (a)University of Applied Sciences Dresden, Department of Electrical Engineering, Friedrich-List-Platz 1, 01069 Dresden, Germany, (b)AMD Saxony LLC & Co. KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Germany

Laser Anneal (LA) is one of the promising technologies for the 65 nm technology node and below. Steep and shallow junctions with a high level of activated dopants are fabricated by using Laser irradiation. The short time at high energy prevents diffusion in the extension and in the poly-silicon gate. However, this causes underlap and gate polysilicon depletion. Another problem might be the high extension sheet resistance due to the shallow junctions, despite of higher doping activation. We show a degradation of the universal curve (Ioff/Ion) for devices with LA in experiments and simulations. An analysis of the possible factors, which are responsible for the universal curve degradation is done by numerical simulations. Adjusting the threshold voltage through the halo implant dose improves the universal curve significantly. We find an increase in saturation current of about 20% at the same off-state current. Other approaches like a deeper source and drain extensions to minimize the sheet resistance or a tilted source and drain extension implant to get more overlap does not affect the universal curve significantly. The CV/I calculation for the LA devices shows a gate delay improvement of the advanced transistor devices. Moreover we have investigated approaches to overcome the problems of laser annealed MOSFETs which are easy to integrate into the current CMOS process.

10:40 **BREAK**

Session II : USJ Formation
Session chair: D. Tsoukalas

D-II.01 11:00 -Invited-

MILLI-SECOND ANNEALING FOR FUTURE CMOS TECHNOLOGIES

M. Foad, Applied Materials, Santa Clara, USA

D-II.02 11:30 -Invited-

ADVANCED ACTIVATION OF ULTRA-SHALLOW JUNCTIONS USING FLASH-ASSISTED RTP

W. Lerch, S. Paul, J. Niess, Mattson Thermal Products GmbH, Daimlerstrasse 10, 89160 Dornstadt, Germany, S. McCoy, T. Selinger, J. Gelpey, Mattson Technology Canada Inc., 605 W. Kent Ave., Vancouver, B.C. V6P6T7, Canada, F. Cristiano LAAS/CNRS, 7 av. Du Col. Roche, 31077 Toulouse, France, P. Pichler, Fraunhofer-IISB, Schottkystrasse 10, 91058 Erlangen, Germany

Advanced-logic device technology for the 65nm node and beyond requires highly-activated, shallow, and abrupt dopant profiles. Combination of ion implantation and advanced annealing technology is expected to provide solutions for these requirements. A diffusion-less but highly activating, high-temperature, flash-assisted RTP annealing approach for the formation of ultra-shallow junctions will be demonstrated which meets the performance specifications for the 65 and 45 nm nodes. In this paper, we will first present some of our recent p+MOS and n+MOS results on the fabrication of ultra-shallow junctions using flash-assisted RTP in crystalline and pre-amorphized silicon. The experimental p+MOS results will be compared to simulations with a predictive model which addresses the diffusion at extrinsic concentrations, the agglomeration of silicon self-interstitials, and the formation of boron interstitial clusters. It was shown already before that this model is able to predict boron diffusion and activation for a wide variety of applications from soak anneals to spike anneals [1]. In the second part, we will present a detailed deactivation study of thermal processes after flash-assisted RTP. Post-annealing temperatures were chosen to “simulate” typical salicide processes for NiSi or CoSi2 contacts in a standard CMOS process flow with annealing times from few seconds up to several hundred seconds. After the post-annealing step, the junctions were analyzed by four point probe measurements, SIMS, TEM and HREM. These results are compared to earlier studies of de-/reactivation phenomena after a 65 nm node solid phase epitaxy growth process [2].

[1] P. Pichler, et al. IEDM Tech. Digest 971-974 (2004)
[2] W. Lerch, et al. Electrochem. Soc. Proceedings 2004-01 p.90-105

D-II.03 12:00

MILLISECOND FLASH ANNEALING: APPLICATIONS FOR USJ FORMATION AND OPTIMIZATION OF DEVICE ELECTRICAL CHARACTERISTICS

G. John Foggiato, Woo Sik Yoo, WaferMasters, Inc., 246 East Gish Road, San Jose CA 95112, USA

To form Ultra Shallow Junctions, USJs, several fast annealing techniques are available for very high temperatures to activate dopants yet minimize diffusion. Flash annealing utilizes Xe-arc lamps which provide a short (2 msec) burst of intense optical energy achieving temperatures in excess of 1350°C. It is shown that this annealing technique facilitates boron activation to its solid solubility level. A detailed review of the flash annealing parameters will describe how they affect leakage currents, junction depths, dopant activation and junction abruptness. To address poly depletion effects, flash annealing can be used to fabricate fully doped poly gates. Several dopants for sub 90 nm devices have been characterized under various annealing conditions resulting in leakage currents comparable to spike anneal and higher current gain. High boron activation concentrations are attained through adjustment of process conditions including modifying the processing sequence by utilizing multiple flash anneals. Certain device geometrical factors and film structures also have to be adjusted to optimally utilize the flash technology with the most important factor being minimization of defect generation with the high energy imparted onto the wafer surface. To control this energy, additional optimization of the flash technology is achievable through varying the energy pulse width and initiation of the Xe-arc lamp ignition. Also discussed are effects on patterned surfaces with different reflectivity and emissivity. Data showing comparative results will be presented, including how such results compare to the use of spike annealing.

D-II.04 12:15

A COMPARATIVE STUDY ON ULTRA-SHALLOW JUNCTION FORMATION USING CO-IMPLANTATION WITH FLUORINE OR CARBON IN PRE-AMORPHIZED SILICON

Houda Graoui, and Majeed A Foad, Applied Materials, Inc., Front End Products Group, 974 E. Arques Ave, Sunnyvale CA 94086, USA

The main driver in ultra-shallow formation for 65 nm technology node and beyond is to find solutions that both reduce boron transient enhanced diffusion and can be integrated in the CMOS process flow. To this end, many studies have recently focused on using co-doping techniques with fluorine and most recently with carbon. In most cases, one or both of these is co-implanted with a dopant specie in pre-amorphized silicon. In this work, we show a comparative study of fluorine or carbon co-implanted with low-energy boron or BF2 to form source and drain extension junctions for PMOS devices. We will show that by a systematic optimization of germanium, boron, BF2, fluorine or carbon energies and doses, spike annealing technology can be extended to the 65 nm node. These results will used to discuss how the different formed junctions offer potential solutions for either low power or high performance PMOS devices fabrication.

D-II.05 12:30

INTEGRATION OF A LONG PULSE LASER THERMAL PROCESS FOR SHALLOW JUNCTION FORMATION OF SUB-45 NM CMOS DEVICES

J. Venturini, M. Hernandez, K. Huet, SOPRA, 26 rue Pierre Joigneaux, 92270 Bois-Colombes, France, C. Laviron, CEA-G / LETI, 17 avenue des Martyrs, 38054 Grenoble Cedex 9, France, H. Akhouayri, Institut Fresnel, D.U. St Jérôme, 13397 Marseille cedex 20, France, T. Sarnet, J. Boulmer, IEF, Bât. 220, Université Paris-Sud, 91405 Orsay Cedex, France

We present results on ultra-shallow junction formation for the sub 65 nm CMOS node by means of a Long Pulse Laser Thermal Process (LP-LTP). Abrupt and ultra-shallow junctions with low resistivities are easily obtained, but the irradiated structures like transistor gates need to be preserved from laser melting. To assess the integration of the laser process in the fabrication of a CMOS device, we studied the influence of two laser process window enlargements. We first use and optimize the explosive crytallization of the doped a-Si arising under a 200ns laser pulse. Then we study the influence of different optical coatings deposited before the laser irradiation. Different materials and coating thicknesses have been evaluated on blanket implanted wafers under a long pulse Excimer laser (308 nm-200ns-15 J) irradiation. The junctions have been characterized by 4-point probe, in-situ reflectivity and transmission electronic microscopy (TEM) pictures. Irradiations have also been performed on coated CMOS structures with 35 nm junctions to assess the integration of the process on a real structure. A selective etching scanning electronic microscope (SEM) view shows that a proper optical coating optimizes the coupling of the deposited laser energy and is promising for improving the integration of the laser activation process of future CMOS junctions.

12:45 **LUNCH**

Tuesday, May 31, 2005 **Afternoon**
Mardi 31 mai 2005 Après-midi

Session III : SOI
Session chair: T. Skotnicki

D-III.01 14:15 -Invited-

STRAIN ENGINEERING IN SOI-TYPE MATERIALS FOR FUTURE TECHNOLOGIES
Bruno Ghyselen, SOITEC, Parc techn. des Fontaines, 38190 Bernin, France
SOI is today the substrate of choice for several applications, including high performance and low power power ICs. Although the adoption of SOI enables extending silicon based IC capabilities, the ITRS roadmap poses additional technological challenges. In order to boost further circuit performance, new solutions are being explored among which increasing the charge carrier mobility has been identified as a requirement. Some solutions to increase mobility are based on local strain that can be induced in Si CMOS transistor channels by transistor manufacturing steps such as nitride spacer deposition or SiGe pockets formation: the so-called "local strain" or "process-induced strain" approach. Several other solutions to increase carrier mobility do exist at the substrate level, independently of transistor geometry. These approaches if necessary can be further combined with "process-induced strain" ones. The attractiveness at the device level of these wafer level based solutions is largely due to their compatibility with standard CMOS integration processes and architectures. Among the different substrate level approaches to increased carrier mobilities in SOI, we will focus here on strained Si layers On Insulator. Different material manufacturing techniques will be considered, and the potential of wafer bonding and layer transfer techniques will be highlighted. An emphasis will be put on strain engineering in SOI layers, focusing on the capability of a wafer bonding interface to maintain the strain initially built in a Si layer, for instance by a preliminary epitaxial growth onto relaxed SiGe layer.

D-III.02 14:45

UNDERSTANDING THE ROLE OF BURIED SI/SIO2 INTERFACE ON DOPANT AND DEFECT EVOLUTION IN PAI USJ
J.J. Hamilton(a), E.J.H. Collart(b), B. Colombeau(a), M. Bersani(b), D. Giubertoni(c), J.A. Sharp(a), N.E.B. Cowern(a), and K.J. Kirkby(a), (a)Advanced Technology Institute, University of Surrey, Guildford, Surrey GU2 7XH, U.K., (b)Applied Materials UK Ltd, Foundry Lane, Horsham, West Sussex RH13 5PX, U.K., (c)Centro per la Ricerca Scientifica e Tecnologia, ITC-irst, Povo, Trento, Italy
P-type ultra shallow junctions (USJ) are widely fabricated using Ge preamorphization (PAI) prior to ultra low energy B implantation. However, for future technology nodes, new issues arise when bulk silicon is supplanted by Silicon-on-Insulator (SOI) [1]. Understanding the strong impact of the buried Si/SiO2 interface, will enable tests of fundamental models on defect evolution, electrical activation and diffusion.
Silicon and 55nm-thick SOITEC(c) SOI wafers were preamorphized with 8keV and 20keV Ge (1E15 cm-2) and implanted with 500eV B (2E15 cm-2). Subsequent to implantation an isochronal annealing study of the samples was carried out. Samples were measured by SIMS, Hall Effect measurements and TEM. The results show a range of effects in both bulk and SOI, including uphill diffusion, TED and deactivation driven by interstitials from end-of-range (EOR) defects, EOR defect evolution and dissolution, and EOR decoration by in-diffused B. Boron deactivates less in SOI material than in bulk silicon and EOR defects are eliminated at lower temperatures in SOI than in the bulk, in cases where the Ge PAI EOR defects are close to the SOI back interface. We will show that this effect arises from competition between the front and back SOI interfaces as sinks for interstitials. Finally, simulations are used to explain and quantify the efficiency of the buried oxide interface in terms of recombination velocity.
[1] C.K. Celler and Sorin Cristoloveanu, J. Appl. Phys., 93, 4955 (2003).

D-III.03 15:00

DOSE LOSS AND SEGREGATION OF BORON AND ARSENIC AT THE Si/SiO2 INTERFACE BY ATOMISTIC KINETIC MONTE CARLO SIMULATIONS
J.E. Rubio, M. Jaraiz, I. Martin-Bragado, P. Castrillo, R. Pinacho and J. Barbolla, Dept. of Electronics, University of Valladolid, 47011 Valladolid, Spain
Continuum downscaling of MOSFET devices requires of ultra-shallow junction formation. Performance of the source and drain from B and As low energy implant and subsequent annealing is seriously affected by the presence of the Si-SiO2 interface. Dopant loss due to segregation and dopant pileup at the interface during TED are crucial phenomena for current and future CMOS devices. In this work we have implemented the Oh-Ward model (1) for the dopant behaviour at the interfaces integrated in an atomistic kinetic Monte Carlo simulator. Dopant traps at the interface can capture from or emit to either side of the interface. Furthermore, segregation of dopants and saturation of the interface by the presence of other species are also included. As a test of the model, boron and arsenic low energy implants through a screen oxide have been simulated. When annealing these very shallow implants, it is observed that the dose needed to saturate the interface and the oxide is comparable to the total implanted dose, in good agreement with experiments. In case of piling-up of dopants at the interface, time evolution of the dopant profiles shows this pileup at short times and the subsequent release of trapped dopants for long time anneals.

D-III.04 15:15

MECHANISMS OF THERMALLY INDUCED DEWETTING OF ULTRATHIN SILICON-ON-INSULATOR

Peter Sutter, Eli Sutter, Center for Functional Nanomaterials, Brookhaven National Laboratory, Upton NY 11973, USA

Mainstream microelectronics has been based predominantly on bulk silicon substrates. Silicon-on-insulator (SOI), a composite material in which a thin monocrystalline Si 'template' is bonded to a conventional Si 'handle' wafer via a layer of amorphous SiO2, has recently been developed into a viable substrate for very-large scale integrated circuits. As a result of these efforts, which were largely driven by the promise of substantial advantages of depleted SOI in high-speed and low-power applications, a first generation of state-of-the-art SOI-based microprocessors has become available commercially.

With the increasing use of SOI in technology, the stability of this material under conditions of thermal and chemical processing needs to be established. As a first step in this direction, we have studied the morphological evolution during annealing of ultrathin SOI with Si template thickness below 10 nm. Annealing at 800?C in ultrahigh vacuum drives the formation of pin holes in the ultrathin Si template, which in turn leads to a controlled dewetting of the monocrystalline Si slab that is strongly affected by its crystallographic structure. We identify the microscopic mechanisms underlying both the dewetting and the spontaneous formation of well-defined Si patterns at deep sub-micron dimensions. Our observations suggest that the dewetting process may not be viewed purely as a parasitic by-product of thermal processing, but could provide a bottom-up approach for controlled deep sub-micron patterning.

D-III.05 15:30

MANUFACTURE AND CHARACTERIZATION OF ALSB SOI MOSFET SELF ALIGNED NANO-TRANSISTORS

M. Derras, A. Kadoun, V. Bayot, Université Djillali Liabes de Sidi Bel Abbes, BP 49 Larbi Ben M'hidi, 22000 Sidi Bel Abbes, Algeria

Several theoretical studies and scaling methods tend to demonstrate that conventional MOSFET architectures fabricated on a bulk silicon substrate will not survive below~50 nm of gate length without a severe degradation of the device performances (control of short channel effect, power consumption, frequency of operation...). Alternative architectures are mainly based on the use of a very thin film SOI substrate (Silicon-On-Insulator): typical active SOI layer thickness ranging between 2 to 20 nm are proposed for 10 to 40 nm gate length MOSFETs. Beyond the introduction of a thin SOI film, MOSFET proposed are based on the accumulation mode with low Schottky barrier (ALSB-MOSFET). The design, optimisation , detailed of fabrication process and electrical and microscopic characterisations of the ALSB-SOI Self Aligned MOSFET Nano-Transistors are the essential objectives of this work. This includes the demonstration of improved performances over conventional MOS architectures: immunity to short channel effects, use of a lightly doped SOI substrate for suppression of the sensitivity to dopant fluctuations in the channel, use of Schottky source/drain (S/D) contacts to suppress issues associated to the tight control of S/D doping and reduced S/D specific contact resistance using Pt silicide.

15:45 **BREAK**

Session IV : Light emitting Si
Session chair: P. Eyben

D-IV.01 16:05 -Invited-

DISLOCATION ENGINEERING FOR Si BASED LIGHT EMITTING DIODES

R. Gwilliam(a), M. Laurenco(a), M. Milosavljvic(a), K.P. Homewood(a) and G. Shao(b)·
(a)Advanced Technology Institute, University of Surrey, Guildford, Surrey GU2 7XH, U.K., (b)School of Engineering, University of Surrey, Guildford, Surrey GU2 7XH, U.K.

Historically, optical functionality in microelectronics has required the use of III-V based optical sources, which are both difficult and expensive to integrate with mainstream silicon processes. While light manipulation and guiding has been demonstrated for some time on silicon platforms, light generation remains elusive. However, within the last few years, efficient silicon based optical sources have started to emerge as viable alternatives to the use of III-V materials. Not only will this produce significant cost savings compared to the use of III-V's, but more importantly, allow for the possibility of full integration within CMOS platforms. One such approach has been the use of "dislocation engineering"; where specific defect structures are created using ion implantation to locally tune the band gap of the silicon, allowing efficient radiative recombination to take place from the p-n junction under forward bias. In this paper, we review the current stage of development of this technology at UniS, focussing on process issues for wavelength tuning and device efficiency and look at the possibilities for utilisation and commercial exploitation of the technology.

D-IV.02 16:35

MODULATION OF THE 1535 NM PHOTOLUMINESCENCE FROM Er DOPED Si-RICH SILICON DIOXIDE BY FIELD-INDUCED QUENCHING

J.M. Sun , W. Skorupa, T. Dekorsy and M. Helm, Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf, P.O. Box 510119, 01314 Dresden , Germany, L. Rebohle and T. Gebel, Nanoparc GmbH, Dresden, Germany

Field-induced quenching of the efficient photoluminescence at 1535 nm was observed from Si-rich SiO2:Er thin films prepared by Er and Si co-implantation. The quenching effect was strongly enhanced by increasing the density of silicon nanoclusters at an electric field above 5 MV/cm. A modulation ratio of 0.37 was obtained at an electric field of 9 MV/cm for a 200 nm Er-doped Si-rich layer containing 0.24 % of Er atoms and 10% excess Si nanoclusters. The mechanism of the field-induced quenching of the photoluminescence was studied by simultaneously measuring the light intensity from nanolusters and Er3+ ions, the injection current and the electric field. The quenching mechanism could be attributed to the field induced separation of the excitons created in silicon nanoclusters and tunneling of carriers between the Er ions and silicon nanoclusters. This strong field quenching effect will be useful for controlling the optical gain in a Si-rich SiO2:Er waveguide amplifiers, but also for the small size optical modulator in silicon photonics.

D-IV.03 16:50

SILICON-BASED LIGHT EMISSION DEVICES

T. Arguirov, M. Kittler, W. Seifert, X. Yu, IHP/BTU Joint Lab, Universitätsplatz 3-4, 03044 Cottbus, Germany and M. Reiche, MPI für Mikrostrukturphysik Halle, Germany

There is substantial need for efficient light emitters in the near IR range that are compatible with standard Si based IC technology for development of on-chip optical interconnects. In this contribution, we deal with both Si based light emission after ion implantation and light emission from a dislocation network formed by direct wafer bonding.

It has been shown, that implantation of B or P in Si leads to anomalous temperature behavior of band-to-band luminescence (increase of intensity with temperature) and causes a significant luminescence at room temperature (EL efficiency > 2%). The origin of this enhancement is not yet fully understood, but probably connected with gettering of impurities in the implanted region quenching non-radiative recombination pathes (e.g. M. Kittler, T. Argirov et al., Optical Materials, in press). The disadvantage of Si-LEDs based on band-band luminescence is the wavelength of about 1.1 µm. For a red shift towards 1.5 µm SiGe could be used. An alternative approach for efficient light emitters involves the radiative D-band recombination of dislocations. Well-defined regular dislocation networks in Si can be produced by wafer direct bonding using a controlled misorientation. Actually, we achieved a sufficiently high dislocation density (20 nm distance between the defects). The dislocation-related D1 luminescence at 1.5µm is well detectable even at room temperature. Another application of such a dislocation network for future bioelectronics might be self organized pattern formation of biomolecules at the Si interface due to Coulomb interaction.

D-IV.04 17:05

ELECTROLUMINESCENCE PROPERTIES of Si MOS STRUCTURES WITH INCORPORATION OF FeSi2 PRECIPITATES FORMED BY IRON IMPLANTATION

C.F. Chow(a,c), S.P. Wong(a,c), Y. Gao(a,c), N. Ke(a,c), Q. Li(b,c), W.Y. Cheung(a,c), M.A. Lourenco(d), K.P. Homewood(d), (a)Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong, China, (b)Department of Physics, The Chinese University of Hong Kong, Hong Kong, China, (c)Materials Science and Technology Research Centre, The Chinese University of Hong Kong, Hong Kon , China, (d)School of Electronics Engineering, Computer and Mathematics, University of Surrey, Guildford, Surrey GU2 7XH, U.K.

Despite the indirect bandgap nature of Si, there has been significant progress made towards a working Si-based light emitting device in the past decade. For example, electroluminescence (EL) at room temperature was recently reported from Si metal-oxide-semiconductor (MOS) structures [1] and room-temperature emission from -FeSi2 LED was also successfully demonstrated [2]. In this work, MOS structures were fabricated on Si with the oxide layer grown by well-controlled rapid thermal oxidation (RTO). Then FeSi2 precipitates were formed inside the MOS active region by iron implantation using a metal vapor vacuum arc ion source at various conditions. EL properties from these FeSi2-Si MOS structures after various thermal treatments were measured as a function of temperature from 80 to 300 K. Our results showed that clear EL signals were obtained even at room temperature for some of the devices prepared at appropriate processing conditions. While in some samples, only a broad emission peak around 1.6 m from the FeSi2 precipiates was observed, in some other samples, both the FeSi2 peak and the Si band edge emission at around 1.1 m were observed. It was also found that there was significant enhancement in the intensity of the Si band edge emission in these Fe implanted structures. Details on the fabrication and thermal treatments of these devices and the dependence of the EL properties on the processing parameters will be presented and discussed. This work is partially supported by the Research Grants Council of Hong Kong SAR (ref. no. CUHK4231/03E), and C. N. Yang Optical Science Fund.

17:30-19:00 **POSTER SESSION I**

in parallel

17:30-19:00 **STUDENT AWARD ORAL SESSION**

Session chair: A.N. Larsen

POSTER SESSION I

Tuesday, May 31, 2005
17:20 – 19:00

Session chair: W. Skorupa

D/PI.01 Leakage Current And Deep Levels In CoSi2 silcided Junction

D. Codegoni, C. De Marco, I. Mica and M.L. Polignano, ST Microelectronics, Via Olivetti 2, 20041 Agrate Brianza (Mi), Italy

It is reported that the CoSi2 formation is associated with a leakage of the source and drain junctions. This phenomenon is ascribed to a localized leakage due to cobalt silicide spikes, or to an effect of the mechanical stress. In this work we show that the junction leakage current is related to the introduction of deep levels in the space charge region of the junction. Both n+/p-well and p+/n-well junctions were studied. The junction active area was defined by the Shallow Trench Isolation, the active oxides were grown and the n+ and p+ regions were obtained by arsenic and boron implantations, respectively. After a recristallization annealing the wafers received a Pre-Amorphization Implantation (PAI). A cobalt layer was deposited and CoSi2 was formed. The leakage currents of both n+/p and p+/n junctions were found to increase when the PAI energy is decreased. The junction reverse current was measured as a function of temperature. Both in low leakage and in high leakage n+/p and p+/n junctions the reverse current shows a relevant generation contribution with about 0.6 eV activation energy. The DLTS spectrum of n+/p junctions was insensitive to the PAI process. On the contrary, the spectra of p+/n junctions showed an electron trap (named E1) located at Et=Ec-0.6eV. The concentration of this level is maximum in the absence of the PAI process and decreases below the detection limit in 40keV PAI energy samples. The location of this level in the energy gap is compatible with the observed reverse current activation energy. By comparing the concentration of the E1 trap with the leakage current of the junctions we conclude that the observed leakage current is due to this midgap level.

D/PI.02 TRAP ANALYSIS IN ERBIUM-SILICIDED SCHOTTKY JUNCTION FOR THE APPLICATION TO DECANANOMETER N-TYPE SCHOTTKY BARRIER MOSFETs

Moongyu Jang, Yarkyeon Kim, Myungsim Jun, Jaeheon Shin and Seongjae Lee, Nano-electronic Devices Team, Future Technology Research Division, Electronics & Telecommunications Research Institute, Daejon 305-350, Korea

Recently, Schottky barrier MOSFETs (SB-MOSFETs) are being studied for the applications in nanometer regime as the alternative of conventional MOSFETs. In SB-MOSFETs, the source and drain are composed of silicide instead of impurity doped silicon. Thus the parasitic resistance can be efficiently eliminated and the process temperature can be reduced lower than 600℃, giving the opportunity to use metal as gate electrode and high dielectric materials as gate insulator. However, in SB-MOSFETs, silicon in channel region reacts with the deposited metals. This reaction can cause the generation of trap states. Thus, for the improvement of the device performance, the interface of Schottky diode should be carefully analyzed. In this work, erbium is chosen as source/drain metal of n-type SB-MOSFETs, because of its low Schottky barrier height for electrons. Erbium silicide is formed on p-type (100) silicon by using rapid thermal annealing technique. Annealing temperature and time is 500℃ and 5 min, respectively. The formation of ErSi1.7 phase is confirmed by x-ray diffraction and Auger electron spectroscopy analysis. The interface of Schottky diode is analyzed using the current-voltage and capacitance-voltage measurement methods by incorporating newly developed equivalent circuit modeling technique. The extracted interface trap density, lifetime and Schottky barrier height for hole are determined as 1.5×10^13 traps/cm^2, 3.75 ms and 0.76 eV, respectively. The interface traps are efficiently cured by N2 annealing and the I-V characteristics of Schottky barrier MOSFETs are dramatically improved. Subthreshold swing and DIBL values are 70mV/decade and 30mV in 100nm gate length erbium silicided SB-MOSFETs with the superior suppression of short channel effects.

D/PI.03 PARAMATERS DEGRADATION OF A POWER VDMOS DEVICE UNDER THERMAL STRESS CONDITIONS

M. Alwan, K. Ketata, LEMI, Rouen University, 76821 Mont Saint Aignan, France

The use of the device under certain operational thermal stress conditions can produce modifications of its physical and electrical properties. Based on the two dimensional simulations and the physics of the device, this paper proposes an analysis of the effect of this type of stress observed on the electrical characteristics of the device. The Parameters responsible of these modifications are determined.

A reduction in threshold voltage correlated to an increase of the thermal stress. the observed degradation is analyzed and a linear degradation curve of the threshold voltage is computed. The output characteristics of the Power VDMOS for different temperatures is related to the degradation of the saturation current. This later is explained by the phenomenon of the carrier mobility modulation in the inversion layer, which can affect the channel resistance. The analysis of the breakdown voltage is performed and an approximate expressions of the ionization coefficient in terms of the temperature, for a range of electric field which is reigning in a functioning plane junction until the breakdown, is proposed. Using the theory of the punch-through junction, the breakdown voltage and space charge extension with respect to the impurity concentration and the temperature is calculated. The capacitances of the device have been studied. We can notice that the drain-gate, drain-source and gate-source capacitances are shifted due to the degradation of device physical properties versus thermal stress.

D/PI.04 FORMATION AND CHARACTERIZATION OF TiSi/SiGeC SCHOTTKY DIODES

K. Ghelamallah, S. Chitroub, BP 111, Village Universitaire de l'USTHB, 16123 Bab Ezzouar, Alger, Algeria

Very thin films of metal silicides play an increasing important role in silicon integrated circuit technology as MOSFETs are shrunk below 0.1 mm of gate length. In order to further pursue down-scaling of MOSFETs in the 10-20 nm range of gate lengths, a significant effort must be devoted to the development of a new architectures based on the low resistivity, and reduced silicide/silicon specific contact resistance. TiSi/SiGeC based silicides is probably the best candidates for that purpose. In this paper, we propose, first provides a detailed analysis of the formation of TiSi/SiGeC silicides. TiSi/SiGeC Schottky diode with an without a Si cap layer are characterised by Rutherford backscatterring spectroscopy (RBS) in order to verify the thickness and composition of silicide phases. The forward and reverse current - voltage (I-V) characteristics dor diodes were measured in the temperature rang of 100 - 300°K to determine the Schottky barrier height and ideality factor. It has been found that the ideality factor decreases with an increase in temperature while the barrier height increases. The effect of the Si cap layer on electrical characteristics of the SiGeC Schottky diodes is also studied.

D/PI.05 SUB 15nm n+/p-GERMANIUM SHALLOW JUNCTION FORMED BY PLASMA DOPING AND EXIMER LASER ANNEALING

Sungho Heo(a), Sungkweon Baek(a), Dongkyu Lee(a), Hyungsuk Jung(a), Geoffroy Raskin(b), Gary Goodman(b) and Hyunsang Hwang(a), (a)Samsung Electronics Co., Giheung-Eup Yongin-City, 449-711, Korea, (b)Umicore Electro-Optic Materials, Watertorenstraat 33, 2250 Olen, Belgium

D/PI.06 EVALUATION OF BBR2 AND B+BR IMPLANTS IN SILICON

J.A. Sharp, R.M. Gwilliam, B.J. Sealy, C. Jeynes, J.J. Hamilton and K.J. Kirkby, Surrey Ion Beam Centre, Advanced Technology Institute, School of Electronics and Physical Sciences, University of Surrey, Guildford Surrey GU2 7XH, U.K.

The International Technology Roadmap for Semiconductors(ITRS) requires the scaling down of the transistors in order for device speeds to meet Moore's law. This scaling includes the source/drain region depths to give ultra shallow junctions(USJ). Ion implantation is the desired method by which to introduce dopant atoms into the silicon to make such regions. To achieve shallower implants, new low energy implanters can be utilised but this is an expensive investment. An alternative is to implant molecular ions containing the required dopant (in this case boron) and other heavier atoms. Currently the molecular boron halide implant of BF2 is used. The presence of fluorine has been shown to increase the activation of the boron after rapid thermal annealing. In the same periodic group as fluorine is bromine. This halide element is heavier than fluorine; therefore shallower implants can be performed with molecular BBr2+ than BF2+ at similar implant energies. Co-implants of boron and fluorine have also been shown to reduce the transient enhanced diffusion of boron during post-implantation annealing. The work carried out here examines the suitability of BBr2+ and B+Br implants into crystalline silicon for USJ applications. Hall effect measurements after rapid thermal annealing have shown a diference in electrical activation between the BBr2+ and B+Br implants. Anomalous hall mobility has also been found for the co-implant and this will be discussed. Rutherford Backscattering Spectroscopy shows that an amorphous region is created during implantation of BBr2+, eliminating the need for a separate pre-amorphising implant. This amorphous region re-grows during subsequent rapid thermal annealing and there is evidence to suggest that the bromine has an effect on the re-growth velocity.

D/PI.07 **D-II.05**

D/PI.08 EXCIMER LASER ANNEALING OF B AND BF2 IMPLANTED Si

E.V. Monakhov and B.G. Svensson, Department of Physics/SMN, University of Oslo, PO Box 1048 Blindern, 0316 Oslo, Norway, M.K. Linnarsson, Solid State Electronics, Royal Institute of Technology, Stockholm, Sweden, A. La Magna, M. Italia and V. Privitera, CNR-IMM, Catania, Italy, G. Fortunato, M. Cuscunà and L. Mariucci, CNR-IFN, Rome, Italy

We have performed a comparative study of B re-distribution and electrical activation after excimer laser annealing (ELA) of B and BF2 implanted Si. B and BF2 were implanted into p-type (100) Si with a dose of 1x1015 cm-2 using energies of 10 keV and 20 keV, respectively. ELA with 1 and 10 pulses was performed in vacuum with samples kept at room temperature and 450oC. Chemical B concentration and electrical activation profiles were measured by secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP), respectively. SIMS data demonstrate that the presence of F does not influence significantly the re-distribution of B during ELA. A build-up in B concentration at the maximum melt depth is observed after ELA with 10 pulses for both the B and BF2 implanted samples. A dramatic contrast, however, can be observed in the electrical activation of the dopant in the B and BF2 implanted samples. While almost 100% electrical activation of B occurs in the B implanted samples, only 20-50% of the dopant can be activated by ELA in the BF2 implanted sample. Possible mechanisms causing the deactivation of B in the BF2 implanted samples after ELA will be discussed.

D/PI.09 CHARACTERISTICS OF SILICON P-N JUNCTION FORMED BY ION IMPLANTATION WITH IN-SITU ULTRASOUND TREATMENT

V.P. Melnik, Ya.M. Olikh, V.G. Popov, B.M. Romanyuk, Yu.V. Goltvyanskii, A.A. Evtukh, Institute of Semiconductor Physics, National Academy of Science of Ukraine, 41 prospect Nauki, 03028 Kiev, Ukraine

The forming peculiarities of electrical active impurities (B, As, Sb) in silicon at in-situ ultrasound (US) excitation have been investigated. The US excitation influences significantly on generated by ion implantation point defect redistribution. It was shown the possibility of control changing the p-n junction parameters by varying the frequency and intensity of US excitation. Such changing is caused by the interaction of Si structural defects with implanted impurity. As this takes place, the changing both the quantity of defects and impurities redistribution are realized at following activation annealing. The influence of US treatment on Si shallow p-n junction parameters has been studied in details. The US defect engineering is perspective at formation of the high quality Si p-n junction.

D/PI.10 MODELING AND EXPERIMENTAL VERIFICATION OF THE 300 MM AR ANNEAL PROCESS

T. Müller, R. Wahlich, P. Krottenthaler, and W. v. Ammon, Siltronic AG, Johannes –Hess-Strasse 24, 84489 Burghausen, Germany, J. Studener, A. Kühhorn, Lehrstuhl SMF, BTU Cottbus, 03046 Cottbus, Germany

State of the art 300 mm wafer have the need for a defect free perfect sur-face layer. Especially the absence of COPs becomes for a large number of CMOS based products an essential issue (like DRAMs, donor wafer for Si-layer transfer technologies, high-end server and processor chips). Fur-thermore the upcoming low thermal budget processes in ULSI technolo-gies need a ready-IG wafer because common oxygen precipitation during the chip manufacturing process chain is not any more possible.

300 mm Argon annealed wafer are an ideal solution for this challenge and deliver a ready IG capability if nitrogen doping is used. To ensure also a cost productive process one has to generate a deep understanding of preventing slip occurrence while keeping high ramp rates in the anneal furnace. A complex interplay of contact-, bending- and thermal stress de-fines proper support geometries to solve the 300 mm slip challenge at process temperatures around 1200°C. The FEM model accuracy of calcu-lating ramp rates was increased by experimentally determining essential material properties like upper yield stress for nitrogen doped silicon and SiC thermal properties for the first time at these high temperatures. The influence of the support geometry on the thermal stress appearance in the supported wafer is strong. Therefore modeling of not only the diffuse but also the specular scattering contributions to the radial radiation transfer mechanism in a vertical batch furnace is of utmost interest.

D/PI.11 STRAIN RELAXATION AND DEFECT FORMATION IN THE STRAINED-Si/RELAXED Si0.78 Ge0.22 /Si (001) HETEROSTRUCTURE

C.H. Jang(a), S.I. Paik(b), Y.W. Kim(b), S.-H. Kim(c), Y.-J. Song(c), N.-E. Lee(a), (a)Dept. of Materials Science and Engineering and Center for Advanced Plasma Surface Technology, Sungkyunkwan University, Suwon,

Kyunggi-do 440-746, Korea, (b)School of Materials Science and Engineering, Seoul National University, San 56-1, Gwanak-gu, Seoul 151-742, Korea, (c)Semiconductor Research Division, Electronics and Telecommunications Research Institute, Taejeon 305-701, Korea
For the practical adoption of strained-Si channels into the nano-CMOS technology below 50 nm technology node, fabrication methods of strained-Si/relaxed SiGe/Si structures and their compatibility with post-thermal processes are to be obtained. In particular, stability of strained-Si channels on relaxed SiGe layers is of great concern because the formation of misfit and threading dislocations and increase of surface roughness can occur during elevated temperature processing due to thermal-induced instability of strained-Si layers. In this study, we investigated thermal stability of strained-Si on relaxed SiGe layer at elevated rapid thermal annealing (RTA) temperatures. Strained-Si channel layers on the relaxed Si1-xGex(x=0.22) buffer layer were deposited by reduced-pressure chemical vapor deposition (RP-CVD). In order to investigate the thermal stability of fabricated strained-Si/relaxed-SiGe/Si(001), RTA treatments were carried out at the temperature range of 700~950 oC in the N2 ambient for 60 sec. Inversion Fourier transformation analysis of the lattice images obtained from the HR-TEM indicated a non-uniform strain relaxation of the strained-Si layers at the RTA temperature  900 oC. Detailed analyses by cross-sectional and plan-view TEM, Raman spectroscopy and atomic force microscope (AFM) showed the formation of many square-shaped pits with the maximum width of  200 nm and the depth of 120 ~ 150 nm. The pit formation on the surface also contributes to the strain relaxation of the strained Si layers in addition to the formation of misfit dislocations and surface roughening. The AEM and XPS analyses of the annealed samples showed a Ge pile-up on the surface as a result of Ge supply from the pit areas.

D/PI.12 NATURE OF THE INTERFACE OF (100)Ge/INSULATOR STRUCTURES WITH ULTRATHIN HfO2 and GeOx(Ny) LAYERS PROBED BY ELECTRON SPIN RESONANCE

A. Stesmans and V.V. Afanas'ev, Department of Physics, University of Leuven, Celestijnenlaan 200D, 3001 Leuven, Belgium
The intense search for the replacement of conventional SiO2 in Si metal-oxide-semiconductor (MOS) technology by an alternative gate insulator has resulted in strong progress in the development of high-k gate dielectrics non-native to Si. As a corollary, new ways are opened to address the application in MOS technology of other semiconductors less fortunate in terms of high quality native insulators. In particular, Ge, and its alloys with Si, have regained interest because of intrinsically higher charge carrier mobility. As known from the standard Si/SiO2-based structures, a prerequisite for device grade MOS entities concerns the tight control of point defects, at the origin of detrimental charge traps. Using the extensive Si/SiO2 knowledge as backdrop, here, we report on an ESR study of occurring point defects in stacks of bulk Ge with nm-thin layers of GeOx, GeOxNy, and HfO2. Particular attention concerns interface defects, with a view to assess the nature of the interfaces comparatively. A main finding is the non-observation of dangling bond (DB) type defects associated with Ge crystal surface atoms, well distinct from the Si/insul-ator case, fated by the archetypal amphoteric Si DB traps (Pb-centers). Only isotropic signals from defects in the near-interfacial Ge oxide or Ge(oxy)nitride layers are observed. Recalling the assumed relationship of DB formation in the Si/SiO2 entity to accommodation of lattice-network mismatch, this points to a fundamental structural difference between the semiconductor/insulator interfaces for Si and Ge, which may ensue repercussions as to the realization of stable device grade interfaces.

D/PI.13 INVESTIGATION OF SI/SIGE/SI ON SI-ON-INSULATOR BY HIGH RESOLUTION ELECTRON MICROSCOPY AND SYNCHROTRON RADIATION DOUBLE CRYSTAL TOPOGRAPHY

T.D. Ma, H.L. Tu, National Engineering Research Center for Semiconductor Materials, General Research Institute for Nonferrous Metals, No. 2 Xinjiekouwai Street, 100088 Beijing, P.R. China, B.L. Shao, A.S. Liu, G.Y. Hu, National Center of Analysis and Testing for Nonferrous Metals and Electronic Materials, General Research Institute for Nonferrous Metals, No. 2 Xinjiekouwai Street, 100088 Beijing, P.R. China
High resolution electron microscopy (HREM) in combination with synchrotron radiation double crystal (SRDC) topography was employed to investigate Si/SiGe/Si on silicon-on-insulator (SOI) subjected to in-situ low-temperature annealing. It has been found that 60o dislocations, dislocation dipoles rarely reported in such SiGe heterostructure and local elastic strain appear in HREM cross-sectional images of the multilayer structure. More defects were observed in the neighborhood of the interface between SiGe layer and the underlying Si layers (including Si buffer layer and top Si layer of SOI) than in that of the interface between SiGe layer and Si cladding. SRDC (004) rocking curves were acquired before and after rotating the specimen 180o around its surface normal. And three peaks due to the diffraction of Si layers, SiGe layer and bulk Si layer were identified respectively. Sharp and faint cross-hatched contrasts were observed in the SRDC topographs of both Si layers and SiGe layer taken at low- and high-angle full width at half maximums (FWHMs). SRDC topographs in comparison with HREM images show that low- and high-angle FWHMs of the Si layers peak should correspond to the diffraction originated from the underlying Si layers and Si cladding. It is the distorted or bended lattice planes besides the finite width of Si layers that make the diffraction peaks of Si layers broaden out into one peak. All results indicate that major strain relaxation happens within the interface between SiGe layer and the underlying Si layers. Strain relaxation does not only depend on formation of 60o dislocations but also on introduction of dislocation dipoles, elastic strain and so on.

D/PI.14 ELECTRON INTERACTION EFFECTS IN STRAINED P-SIGE/GE HETEROSTRUCTURES

B. Rössner, B. Batlogg, Laboratory of Solid State Physics, ETH Zurich, 8093 Zurich, Switzerland, H. von Känel, D. Chrastina, G. Isella, INFM and L-NESS, Dipartimento di Fisica del Politecnico di Milano, Polo Regionale di Como, Via Anzani 52, 22100 Como, Italy
The highest low-temperature hole mobilities in the SiGe material system have been reported from compressively strained Ge channels on thick, relaxed graded buffers. The samples were grown by low-energy plasma-enhanced chemical vapor deposition (LEPECVD) [1].
Here, we report on the low field magnetoresistance of such structures as function of carrier density (1 - 5x10^11 cm^-2) and temperature (0.5 - 20 K). Modulation of the carrier density was achieved both by application of a gate voltage and illumination of the samples at liquid helium temperatures. The density dependent mobilities range from 5000 to 50000 cm^2/Vs, where high mobilities are associated with high carrier densities. The carrier density was determined from the Hall effect. Interpreting the magnetoresistance in terms of electron-electron interaction and Zeeman effects as well as weak localization allow to determine the relevant scattering times and the Fermi liquid parameter F*. The functional form of the magnetoresistance fits theory well. At low densities, e-e interaction seems to dominate while at higher densities the Zeeman contribution plays an important role. For sheet carrier densities above 5x10^11 cm-2 the corrections are no longer observable while the mobility rises up to 120 000 cm^2/Vs [2]. [1] H. von Känel et al, Appl. Phys. Lett. 80, 2922 (2002) [2] B. Rössner et al, Appl. Phys. Lett. 84, 3058 (2004)

D/PI.15 RAMAN SPECTROSCOPY OF Si1-xGex EPILAYERS

F. Pezzoli, Lucio Martinelli, E. Grilli, M. Guzzi, S. Sanguinetti and M. Bollani, INFM and L-NESS, Dipartimento di Scienza dei Materiali della Università degli Studi di Milano-Bicocca, Via Cozzi 53, 20125 Milano, Italy, H.D. Chrastina, G. Isella and H. von Känel, INFM and L-NESS, Dipartimento di Fisica del Politecnico di Milano, Via Anzani 52, 22100, Como, Italy, E. Wintersberger, J. Stangl and G. Bauer, Institute for Semiconductor Physics, J.-Kepler University Linz, Altenbergerstr. 69, 4040 Linz, Austria

The first systematic investigation of the vibrational properties of epitaxial Si1-xGex alloys in the composition range 0≤x≤1 is presented. A Raman spectroscopy study has been undertaken in order to investigate the phonon mode frequency dependence on structural and elastic parameters such as Ge concentration, strain relaxation and clustering effects in the alloys. The samples, consisting of thick Si1-xGex cap layers on top of graded alloys, were grown with Low Energy Plasma Enhanced Chemical Vapour Deposition (LEPECVD), an innovative growth system which overcomes many limitations of the conventional epitaxial techniques.
Reciprocal Space Mapping measurements confirmed that SiGe alloys grown by LEPECVD on virtual substrates are relaxed and provided the alloy composition. High resolution Raman measurements allowed us to determine very accurately the dependence of the phonon modes on the composition of relaxed SiGe alloys. Furthermore, our results demonstrate that in the LEPECVD grown alloys the presence of clustering or ordering effects is very unlikely and thus these materials are purely statistical alloys in the whole composition range.

D/PI.16 SN-BASED GROUP-IV SEMICONDUCTORS ON SI: NEW INFRARED MATERIALS AND NEW TEMPLATES FOR MISMATCHED EPITAXY

John Kouvetakis and Jose Menendez, Arizona State University, Tempe AZ 85287-1504, USA

We report on the growth and properties of binary GeSn and ternary SiGeSn alloys on Si substrates. Using a novel CVD approach, high quality GeSn films have been deposited on Si substrates. X-ray studies indicate that the films are strain-free, and electron microscopy results show that the large lattice mismatch between the film and the substrate is relieved by Lomer dislocations at the interface. The bulk of the films are found to be virtually dislocation free. This material is of great interest due to the predicted cross-over to a direct gap semiconductor for moderate Sn concentrations. We have carried out extensive optical studies, including spectroscopic ellipsometry, to study its electronic structure.
The ternary SiGeSn alloy has been grown for the first time on GeSn buffer layers. This material opens up entirely new opportunities for strain and band gap engineering using group-IV materials. In particular, we have shown that it may be possible to design multilayer systems containing Ge layers with a strain-induced direct band gap. In addition to acting as a buffer layer for the growth of SiGeSn, we have found that GeSn can act as a template for the subsequent growth of a variety of materials, including SiGe and III-V semiconductors.

D/PI.17 LOW ELECTRICAL RESISTIVITY POLYCRYSTALLINE SIGE FILMS OBTAINED BY VERTICAL LPCVD FOR MOS DEVICES

R.C. Teixeira, I. Doi, M.B.P. Zakia, J.A. Diniz, J.W. Swart, School of Electrical and Computer Engineering (FEEC) and Center for Semiconductor Components (CCS), State University of Campinas (UNICAMP), P.O. Box. 6061, CEP 13083-870, Campinas-SP, Brazil

Silicon Germanium alloys (SiGe) have presentely been used in several microelectronic devices due to their enhanced electrical properties. In this study, authors present some morphological and electrical characterization of polycrystalline SiGe thin films (poly-SiGe) deposited by LPCVD in a vertical (pancake) reactor, aiming for gate electrode in MOS devices. Precursor gases were SiH4 and GeH4 in a H2 carrier gas flow. Deposition temperature ranged from 500 to 750 °C, with 50 °C steps, at 5 or 10 Torr pressure.
The obtained samples are very uniform, with less than 1% deviation (std. dev./mean thick) in a 1x1 inch area for all samples and AFM measurements showed a smooth surfaces (rms roughness as low as 4 nm for sample deposited at 550 °C / 10 Torr can be achieved) and grain size of about 50 nm. The deposition process is thermally activated and high deposition rates (up to 150 nm/min) are achieved. Changes in deposition temperatures lead to a different internal structure of the samples observed by XRD measurements. 5 Torr samples exhibit a stronger <111> preferred orientation (PO) as temperature raises while 10 Torr samples presents <111> PO only at 750 °C. At lower temperatures, poly-SiGe films deposited at 10 Torr presents a <220> PO. Different Ge concentrations are also achieved raising rapidly up to a maximum of about 30% and 37% Ge fraction at 600 °C for 5 and 10 Torr respectively. Above this temperature, Ge fraction decreases slowly to 25% Ge for both 5 and 10 Torr pressure. Its seems that these results of PO and Ge fraction are not correlated. A second set of samples was also prepared to analyze some poly-SiGe electrical properties. The results are compared to similar thickness poly-Si films obtained at the same reactor. We found that resistivity values as low as 0.42 mohm.cm can be achieved in phosphorus-implanted poly-SiGe films. This value is one order of magnitude lower than the obtained in poly-Si at the same doping conditions. Actually, a 500°C rapid thermal annealing can lead to poly-SiGe thin films with one-third the resistivity of poly-Si films annealed at 900°C, using the same implantation dose.

D/PI.18 INTRINSIC STRESS IN AMORPHOUS AND NANOCRYSTALLINE Si FILMS PREPARED BY PECVD WITH HYDROGEN DILUTION

Y.Q. Fu, J.K. Luo, S. Milne, A.W. Flewitt, W.I. Milne, Department of Engineering, University of Cambridge, Trumpington Street, Cambridge CB2, 1PZ, U.K.

Amorphous and nanocrystalline hydrogenerated silicon films have been attractive for the potential applications in solar cells, thin films transistors in liquid crystal displays and Si based optoelectronics devices. In this study, amorphous and nanocrystalline Si films were prepared using radio-frequency (13.56 MHz) plasma enhanced chemical vapour deposition with different SiH4/H2 ratios. The film residual stress was measured using curvature methods as a function of hydrogen dilution ratio, and then the intrinsic stress was obtained with the deduction of thermal stress. The film intrinsic stress was analyzed in details correlated with films properties (hydrogen contents in films, hydrogen bonding conditions, optical properties, crystallite size and ratio in amorphous matrix). Results revealed that the intrinsic stress of amorphous Si films changed from tensile to compressive with the increase in plasma power. With a fixed power and gradual introduction of hydrogen dilution, the film intrinsic stress increases significantly until with a hydrogen dilution ratio of 98%. Above that critical ratio, the film intrinsic stress decreases sharply. Different mechanisms of stress formation and relaxation during film growth were discussed, including ion bombardment effect, hydrogen induced bond-recontruction, nanocomposite effects (nanocrystal with different sizes and ratio embedded amorphous Si matrix), etc. The mechanical properties (modulus and hardness) of the films were also characterized and correlated with film stoichiometry and microstructure and stress.

D/PI.19 THE FEATURES OF THE FORMATION OF SiGe NANOISLANDS ON SiGe BUFFER

M.Ya. Valakh, V.M. Dzhagan, O.S. Lytvyn, A.M. Yaremko, V.O. Yukhymchuk, Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine, Prospekt Nauki 41, 03028 Kyiv, Ukraine, Z.F. Krasil'nik, A.V. Novikov, Institute for Physics of Microstructures RAS, 603950 Nizhny Novgorod, GSP-105, Russia

The SiGe nanoislands formed on a strained Si0.9Ge0.1 buffers by various thickness of deposited Ge at 700oC are studied by atomic force microscopy and Raman scattering. The obtained nanoisland's characteristics are compared with typical ones of nanoislands grown on Si buffer. The morphology of these two systems differs dramatically: an increase in both the surface density and sizes of the islands were noted. For islands grown on the Si0.9Ge0.1 buffer, we also established an increase in a critical volume at which a pyramid-to-dome transition occurs. This result is explained as due to the increase of Si content in the islands at the very early stage of the growth. The strain and composition in the islands formed on Si and Si0.9Ge0.1 buffers were determined from the Raman spectra. Additionally, we discuss the degree of strain relaxation caused only by the three-dimensional islands geometry.

D/PI.20 STRAIN AND DEFECT ENGINEERING IN Si/Si3N4/Si BY HIGH TEMPERATURE – PRESSURE TREATMENT

A. Misiuk, A. Barcz, Institute of Electron Technology, Al. Lotnikow 46, 02-668 Warsaw, Poland; B. Surma, IEMT, 01-919 Warsaw, Poland; I.V. Antonova, ISP RAS, 630090 Novosibirsk, Russia and S. Dub, ISM, 04074 Kiev, Ukraine

Strain and defects in SOI-like structures prepared by N2+ implantation into Si are dependent on hydrostatic pressure (HP) of ambient applied at annealing of Si:N [1]. This effect of HP is now investigated in more details.
Cz-Si wafers were implanted with N2+ (doses 1x1017 or 1x1018 cm-2, E = 140 keV) and treated for 5 h in Ar atmosphere at up to 1400 K under HP up to 1.2 GPa. Next the Si/Si3N4/Si samples were investigated by SIMS, photoluminescence (PL), electrical and related methods. The treatments at £ 920 K - HP resulted in PL at 0.78 eV; the intensity of PL increased with HP. The dislocation - related PL lines at 0.81 eV and 0.87 eV were observed for Cz-Si:N treated at (1070 - 1270) K - HP, but not at 1400 K - HP. Micro-hardness of Si/Si3N4/Si increased with HP. Effective thickness of buried Si3N4 in the SOI-like structures formed at high temperatures, decreases with HP. Gettering of defects from the surface Si layer to buried Si3N4 takes place so the near surface Si layer of high perfection is formed. Pressure - induced changes of the fixed charges in Si3N4 are related to the HP induced misfit at the Si/Si3N4/Si interfaces. 1. J. Bak-Misiuk, A. Misiuk, W. Paszkowicz, A. Shalimov, J. Hartwig, L. Bryja, J.Z. Domagala, J. Trela, W. Wierzchowski, K. Wieteska, J. Ratajczak, W. Graeff, J. Alloys Comp. 362 (2004) 275.

D/PI.21 WAFER BONDING INVOLVING STRAIN-RELAXED SiGe

I. Radu, R. Singh, M. Reiche, U. Gösele and S.H. Christiansen, Max Planck Institute of Microstructure Physics, Weinberg 2, 06120 Halle/Saale, Germany

Strain-relaxed SiGe grown on silicon form virtual substrates for the deposition of strained silicon (sSi) as active device channels with enhanced carrier mobility compared to bulk Si. The relaxation of the SiGe is mediated through misfit dislocations near the SiGe/Si interface that are however, connected to the free surface by dislocation segments threading through the layer. These threading dislocations (TDs) running through the active device channel may deteriorate device performance. The density of TDs is reduced by either compositional grading of the SiGe layer (few µm thick) or by relaxation of a thin pseudomorphic SiGe layer (<500 nm) through hydrogen/helium implantation and subsequent annealing. The latter type of substrates shows a much lower surface roughness (root mean square (RMS) <1 nm), while the graded virtual substrates show a cross-hatch pattern on the surface that gives rise to a RMS value >1 nm. Wafer bonding is then used to attach the sSi or the relaxed SiGe layer to an oxidized handle wafer to create sSi-on-insulator (sSOI) and silicon-germanium-on-insulator (SGOI). In this paper we report wafer bonding of different virtual substrates and sSi layers. For a successful bonding the cross-hatched substrate needs surface planarization e.g. chemo-mechanical polishing which can be combined with oxide deposition. We will discuss the bonding behavior of various deposited oxide layers, such as plasma enhanced (PE)-CVD, PE-TEOS, high density plasma (HDP)-CVD and thermal oxides on sSi layers (residing on different virtual substrates). The quality of the bonded interface is assesed by infrared (IR) microscopy and bond strength measurements. Cross-sectional transmission electron microscopy is used for the microstructural characterization of the bonded interface.

D/PI.22 FORMATION OF SILICON-ON-DIAMOND-LIKE-CARBON NOVEL STRUCTURE BY ION CUTTING AND SIMULATION OF SELF-HEATING EFFECTS

Chenglu Lin(a), Ming Zhu(a), Weili Liu(a), Zengfeng Di(a,b), Paul K. Chu(b), (a)Research Center of Functional Semiconductor Film Engineering & Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, 865 Changning Road, 200050 Shanghai, China, (b)Department of Physics and Materials Science, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong

Silicon-on-insulator (SOI) microelectronic devices suffer from an inherent self-heating effect due to the low thermal conductivity of the buried oxide layer in conventional SOI devices. We propose to replace the buried SiO2 layer in silicon-on-insulator with a plasma synthesized diamond-like-carbon (DLC) thin film to mitigate the self-heating effects. Atomic force microscopy (AFM) results indicate that the DLC films exhibit outstanding surface topography due to our special plasma implantation process. The optimal ion energy creates good film adhesion as well as excellent surface flatness. The DLC films also show excellent insulating properties up to an annealing temperature of 900ºC. Hence, the degree of graphitization in our DLC materials is insignificant during thin-film transistor processing and even in most annealing steps in conventional CMOS processing. Then, using Si/DLC direct bonding and the hydrogen-induced layer transfer method, a silicon-on-diamond (SOD) structure has been fabricated. Cross-sectional high-resolution transmission electron microscopy reveals that a uniform buried DLC layer beneath a Si overlayer that exhibits nearly perfect single crystalline quality. The interfaces between the top Si layer, buried DLC layer, and Si substrate are smooth and sharp. A model is postulated to describe the reactions occurring at the interface during the annealing steps in Si-DLC wafer bonding. In addition, using a two-dimensional device simulation program Medici, the high-temperature operation of MOSFETs fabricated in SOD substrate is investigated. The performance of the SOD device is compared to that of SOI and bulk Si MOSFETs and it is found that the self-heating penalty of SOI can indeed be mitigated using SOD substrate.

D/PI.23 A NEW PROCESS FOR THINNING OF SOI SUBSTRATES BASED ON HCL ETCHING USING RPCVD REACTOR

J. Hållstedt, and H.H. Radamson, Royal Institute of Technology (KTH), Department of Microelectronics and Information Technology (IMIT), Electrum 229, Kista-Stockholm, 164 40, Sweden

The use of SOI wafers has increased rapidly in the recent years. The applications of these substrates demand a thickness range for the Si top layer from a couple of nanometers to some micrometers. Usually an oxidation step with a subsequent HF dip or chemical mechanical polishing (CMP) are applied to reduce the Si layer thickness, however, these lead to a long-time process. Moreover, the generation of defects in the Si layer after these processings is inevitable. In this article, a novel process based on HCl etching and/or epitaxy of SOI substrates (smart-cut and SIMOX) in a RPCVD reactor is proposed which is a few minutes process with excellent control. Si or SiGe epitaxial layers have been grown on SOI substrates directly after etching of the Si top layer. Temperature dependency of HCl etching and integration of epitaxy have been investigated. Issues e.g. defect generation, surface morphology, layer uniformity and process reliability have been studied.

In extension, HCl etching has been applied on the patterned SOI substrates for formation of defect free Si wires or pillars. This method enables for a lateral epitaxy for these formed structures. High-resolution X-ray diffraction has been applied to measure the layer thickness. Smart-cut SOI substrates shows both tilt and twist of the Si top layer compared to the Si bulk. Meanwhile the X-ray analysis becomes more difficult for SIMOX substrates specially for thin Si cap layers. This is due to the overshadowing of the high intensity Si bulk peak on the Si top layer. In this case, a triple axis configuration in the secondary optics of X-ray instrument is necessary to decrease the diffracted divergency.

D/PI.24 PRECISE CHARACTERIZATION OF SILICON ON INSULATOR (SOI), SiGe ON SOI (SGOI), AND STRAINED SILICON ON INSULATOR (SSOI) STACKS WITH UV-VISIBLE – INFRA RED SPECTROSCOPIC ELLIPSOMETRY

Adrien Darragon, Christophe Defranoux, Thierry Emeraud, Jean-Louis Stehle, SOPRA SA, Bois Colombes, France

Further improvements in CMOS circuit performance such as switching speed and power reduction will rely on the use of silicon on insulator (SOI) substrates with decreased functional thicknesses. According to the International Technology Roadmap for Semiconductors (ITRS), the silicon and buried SiO2 (BOX) layer thicknesses for a fully depleted device should be in the ranges of 10 - 16nm and 24 - 40nm by 2005, respectively. A key issue for fully depleted CMOS transistors is the control of such ultra-thin layers thickness and their uniformity with other parameters such as surface and interface roughness. This is a challenge to metrology, especially to conventional reflectometry technique because the layers thickness must determined with angstrom precision for both silicon cap and SiO2 box layer.

Spectroscopic ellipsometry (SE) is an optical and non-destructive technique for determining thin film thickness and material optical properties. Because ellipsometry measures change in the polarization state for both the amplitude ratio of the p to s polarizations, and in phase retardation, it provides a precise way to characterize such ultra thin SOI stacks (10 - 20nm). Comprehensive characterization results for a number of thin and ultra thin SOI stacks with different thickness ranges will be presented together with measurement repeatability results relevant to the film thickness process tolerances.

In addition, characterization results for advanced device applications such as SiGe on SOI (SGOI) and strained silicon-on- SiGe-on-insulator (SSOI) will be shown, demonstrating the use and capability of spectroscopic ellipsometry for precise determination of layer thickness, material composition, interfacial layers, etc.

SiGe/Si heterostructure provides a way to improve silicon based device performance through modification of the band gap and band alignment. The ability to precisely determine epilayer thickness and Ge concentration is essential for calibrating growth processes and thus control film quality. Spectroscopic ellipsometry is a non-destructive optical technique and has advantages for in-line process monitoring over SIMS, TEM and other destructive techniques. With integrated UV-Vis-IR spectroscopic ellipsometer, not only epilayer thickness and Ge concentration can be obtained with the UV-Vis channel, but also p-type dopant concentration with the IR channel, These parameters are measured on both Si or SOI substrates (SGOI). In this presentation, an alloy model will be introduced first to obtain Ge concentration. Metrology of other advanced Substrates such as the characterization of very thin Silicon Epi layers, SIC, Silicon on Sapphire (SOS) will also be presented. Principles and advantages of the technique will also be discussed in the presentation.

D/PI.25 DEFECT ENGINEERING FOR ION BEAM SYNTHESIS OF SILICON-ON-INSULATOR STRUCTURES

R. Kögler, F. Eichhorn, A. Mücklich, H. Reuther, W. Skorupa; Forschungszentrum Rossendorf, FWI, PF 510119, 01314 Dresden, Germany

Silicon-on-insulator (SOI) is a substrate material used for the fabrication of high-speed devices. A buried insulating SiO2 layer is synthesized by high-temperature, high-dose oxygen ion implantation into crystalline silicon and subsequent thermal treatment. The intention of this ongoing study is the application of defect engineering methods for the reduction of the oxygen ion dose and the improvement of the crystal quality in the resulting top-Si-layer.

The oxygen ion dose can be reduced by the pre-deposition of gettering centres for the implanted oxygen which are introduced by He or Si implantation. Moreover, a fraction of the necessary oxygen dose is replaced with controlled surface oxidation and the corresponding oxygen migration toward the buried SiO2 layer. The implantation damage in the top-Si-layer is diminished by in-situ introducing of (i) vacancies in the O-implanted region to accommodate interstitials ejected from volume expansion by SiO2 formation and of (ii) interstitials into the top-Si-layer to recombine implantation induced excess vacancies. In-situ defect engineering during implantation is performed in the Rossendorf dual implantation chamber (DIC). This equipment enables the simultaneous implantation with two scanned ion beams in synchronized mode. Analysis results of the SOI structures obtained by TEM, SRP and XRD will be presented.

D/PI.26 FABRICATION OF SILICON ON INSULATOR WITH BURIED TUNGSTEN SILICIDE LAYER FOR HIGH FREQUENCY INTEGRATED CIRCUITS

Weili Liu(a), Suhua Luo(a,b), Miao Zhang(a), Zhitang Song(a), Chenglu Lin(a), Paul K. Chu(b), Xiaolan Liu(a), (a)Research Center of Functional Semiconductor Film Engineering and Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, 865 Changning Road, 200050 Shanghai, China, (b)Department of Physics and Materials Science, City University of Hong Kong, Tat Chee Avenue, Koloon, Hong Kong

In mixed-mode high frequency integrated circuits the coupling of signals through the substrate is a major problem. For operating frequencies below 10GHz SOI substrates offer better protection against cross-talk, but at higher frequencies the buried oxide becomes transparent to the signals. A high conductive layer below the buried silicon

dioxide layer can be used as a ground plane to pin potential on the surface of the handle wafer. Cross-talk will therefore be suppressed since lateral potential variations are eliminated. In this work, single-crystalline Si/SiO2/poly-WSix/Sub-Si structure has been successfully fabricated by a new method incorporating smart-cut technology and high temperature reaction between tungsten and silicon. The tungsten silicide in our work is formed by the reaction of tungsten and silicon during high temperature annealing, before which smooth amorphous W and Si layers were deposited on a bare Si wafer in turn and then it was bonded with a hydrogen-implanted silicon wafer with a SiO2 layer on the surface. After annealed at 800-1100℃, a poly-crystalline WSix (1<x<2) layer with tetragonal structure is formed below the buried oxide layer. Cross section images of TEM show three steep interfaces of four layers. It is found that increasing annealing temperature can decrease sheet resistance of tungsten silicide and improve the crystal quality of the top silicon layer. But spreading resistance profile measurement also shows that annealing under high temperature (≥1000℃) will induce diffusion of tungsten into Si substrate which is confirmed by EDX result. Our experiment shows that combining the Smart-Cut technique with solid phase reaction provides a novel method to make the buried tungsten silicide ground plane.

D/PI.27 HIGH-GERMANIUM RELAXED SiGe-ON-INSULATOR FABRICATED BY DRY OXIDATION OF SANDWICHED Si/SiGe/Si STRUCTURE

Zengfeng Di(a,b), Miao Zhang(a), Weili Liu(a), Ming Zhu(a,b), Chenglu Lin(a), and Paul K Chu(b), (a) The Research Center of Semiconductor Functional Film Engineering Technology & State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS), Shanghai 200050, People’s Republic of China, (b)Department of Physics and Material Science, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong, China

We have developed an improved technique to fabricate silicon-germanium on insulator (SGOI) starting with a sandwiched structure of Si/SiGe/Si. By means of oxidation and annealing, relaxed SiGe-on-insulator (SGOI) with a Ge fraction of 18% has been produced. Our results indicate that the formation of silicon dioxide suppresses Ge loss at the initial stage of the SiGe oxidation and the subsequent annealing process homogenizes the Ge fraction and also reduces Ge enrichment under the oxide. Raman measurements reveal that the strain in the SiGe layer is fully relaxed at high oxidation temperature (~1150oC).

D/PI.28 WITHDRAW

D/PI.29 ELECTRICAL CONDUCTIVITY ACROSS THE BONDED INTERFACE IN UNIPOLAR Si/Si JUNCTIONS AT T=78 AND 300 K

V.A. Stuchinsky and G.N. Kamaev, Institute of Semiconductor Physics, 13 Lavrent’ev Ave., 630090 Novosibirsk, Russia

The improved characterization procedure of [1] was used to examine the electrical state of directly bonded p-Si/p-Si junctions with NB"1×1015 cm-3 at T=300 and 78 K. The approach of [1] is based on representation of a real bicrystal structure, whose interfacial potential barrier continuously fluctuates over the junction area, with an equivalent structure consisting of two areal parts, a barrier one with a laterally uniform interfacial barrier and quasi-ohmic interfacial "punctures". In [1], it was shown possible to determine, based just on measured integral (IV and CV) characteristics of real junctions, the contributions of the two areal parts to the total electrical conductivity across equivalent structures and calculate, with due regard for the leakage current through "punctures", the doping profile of the semiconductor and the (effective) energy spectrum of interfacial states (IS) at the junction interface. In the present study, we give a comprehensive comparative analysis of the electrical state of examined junctions at T=78 and 300 K, showing that in both cases the conduction through punctures prevails in their total transversal conductivity, which fact explains weak temperature dependence of typical electric currents and characteristic frequencies at which the junction capacitance displays a frequency-dependent behavior due to IS.

[1] Stuchinsky V.A., Kamaev G.N. Electrochemical Society Proceedings, PV-2003-19 Semiconductor Wafer Bonding VII: Science, Technology, and Applications, 2003, pp. 203-211.

D/PI.30 ELECTROREFLECTANCE SPECTROSCOPY STUDY OF ULTRATHIN SiO2 LAYERS GROWN ON HYDROGENATED SILICON

A. Szekeres(a), R. Holiney(b), S. Alexandrova(a), L. Matveeva(b), (a)Institute of Solid State Physics, 72 Tzarigradsko Chaussee, Sofia 1784, Bulgaria, (b)Institute of Semiconductor Physics, Prospect Nauki 45, Kiev 252028, Ukraine

In Si-based technology for future MOS devices the conditions of Si surface will play the most decisive role influencing the growth kinetics and properties of ultrathin SiO2 layers. Recently, chemical wet and dry plasma treatments of Si surfaces have focused much attention in relation to the subsequent thermal oxidation. We have applied rf hydrogen plasma cleaning of Si and we have established that, in comparison to standard RCA cleaned Si, incorporated hydrogen in the Si surface region helps the growth of more perfect SiO2 network at temperature as low as 800oC. We suggest that, if the amount of hydrogen in the Si surface region is increased, the oxidation temperature could be further lowered growing oxides with similar properties. This could be achieved by applying plasma immersion implantation technique.

In this paper we present results on the study of the thin SiO2 layers grown on Si, hydrogenated by plasma immersion ion implantation technique. The ion energy was 2 keV and the ion dose varied from 10e13 to 10e15 cm-2. The oxidation was performed at temperatures of 700 and 750oC. The oxides were studied by electroreflectance spectroscopy being highly sensitive to the electron states at the material surfaces and interfaces. Our earlier electroreflectance studies on oxides, grown on hydrogen plasma cleaned Si, have shown that the amount of hydrogen strongly affects the oxide stress level and interface defect density. From the electroreflectance spectra analysis the Si energy band and broadening parameter have been elaborated. The results have shown that the oxide stress depends on the hydrogen dose and the oxidation temperature. The built-in stress levels have been inferred and it has been shown that at certain conditions oxide grows in almost stress free conditions.

D/PI.31 STRUCTURE OF THE SiO2/Si-INTERFACE IN DEPENDENCE ON THE SURFACE ORIENTATION OF THE Si-SUBSTRATE

S. Dreiner, M. Schuermann, U.Berges, C. Westphal, University of Dortmund, Otto-Hahn-Str. 4, 44221 Dortmund, Germany

Photoelectron diffraction is one of the few diffraction techniques which require no long range order to get information about the local atomic structure. Therefore, this technique is a perfect tool to investigate the transition between crystalline silicon and its amorphous oxide. The investigated SiO2/Si interfaces were

produced by thermal oxidation of silicon with various surface orientations (Si(100), Si(111), Si(110)). High resolution photoemission spectra of the silicon 2p core-level with a photon energy of 180 eV were recorded at the U-41-PGM beamline at BESSY II. The line-shape consists of several resolved components, which correspond to the electron signals of unoxidized Si (Si_0) and the various different oxidation states of silicon (Si_1+, Si_2+, Si_3+, Si_4+). The population and depth distribution of the different suboxide species are obtained by analyzing the Si_x+ photoemission intensity as function of the polar angle. The analysis of the Si_x+ diffraction patterns provides additional information about the local atomic structure of each suboxide. We compare the results of the different surface orientations.

D/PI.32 THE EFFECT OF TEMPERATURE ON CAPACITANCE-VOLTAGE (C-V) CHARACTERISTICS OF SIMOX

Ahalapitiya H. Jayatissa and Zhiyu Li, MIME Department, College of Engineering, The University of Toledo, OH 4600, USA

Silicon implanted by oxygen (SIMOX) has been proposed for many applications such as floating quantum dot, MOS and MEMS devices. The temperature dependence of interlayer capacitance is one of the most important factors for determining the reliability of SIMOX in practical applications. We have investigated the effect of temperature on Capacitance-Voltage (C-V) Characteristics of SIMOX The capacitance structure were made by etching and coating of Al contact on n-type SIMOX wafers with 157 nm thick buried oxides. The capacitance between top-Si and bulk Si region was defined by microlithography. The temperature were controlled from 0-150 degree C. The results were obtained a function of measured temperature as well as contact electrode materials. A qualitative and quantitative analysis of C-V characteristics will be presented.

D/PI.33 LIGHT EMITTING NANO-POROUS SILICON STRUCTURES FABRICATED USING A PLASMA HYDROGENATION TECHNIQUE

Y. Abdi(b), J. Derakhshandeh(a), S. Mohajerzadeh(a), F. Nayeri(a), E. Arzi(b) and M.D. Robertson(c), (a)Thin Film Lab, University of Tehran, Tehran, Iran, (b)department of physics, University of Tehran, Tehran, Iran, (c)Department of Physics, Acadia University, Nova-Scotia, Canada

D/PI.34 IMPLANTATION OF B AND P IONS IN Si NANOSTRUCTURES WITH SUBSEQUENT THERMAL AND LASER ANNEALING

G.A. Kachurin(a), S.G. Cherkova(a), V.A. Volodin(a), D.V. Marin(a), A.K. Gutakovsky(a), D.I. Tetelbaum(b), H. Becker(c), (a)Institute of Semiconductor Physics SO RAN, 630090 Novosibirsk, Russia, (b)NIFTI, Nizhegorodsky State University, 603950 N. Novgorod, Russia, (c)Laser Centrum Hannover e.V., 30419 Hannover, Germany

Light emitting Si nanocrystals (Si-ncs), synthesized in SiO2 layers, were implanted with 1013-1016cm-2 B or P ions. The post-implantation heat treatments were performed by the 30 min furnace annealing up to 1100oC, or by the 20 ns laser pulses. Photoluminescence (PL), Raman spectroscopy, and HREM were used for characterizations. The low dose implantations have shown even individual displacements in Si-ncs quench their PL. The comparison of elastic energy losses for B and P ions with those known for He ions gave the inverse dependence of the PL quenching on particle masses. This may be explained by a growing binding of mobile defects. Restoration of PL from partly damaged Si-ncs proceeds at annealing <1000oC. In the low dose implanted and annealed samples an increased Si-ncs PL was found and ascribed to the radiation-induced shock crystallization. After implantation of high doses an enhanced recovery of Si-ncs was observed for the impurity concentrations >0.1 at.%. The effect resembles the impurity-enhanced crystallization, known for bulk Si. Fully amorphized nanoinclusions need ~1100oC anneals to be re-crystallized. Owing to the difference in the atomic sizes, B-doped Si-ncs were less perfect than P-doped ones, and needed higher annealing temperatures. The 300-mJ/cm2 laser pulses gave better results than 1100oC furnace anneals, supposedly due to short time melting. The impurity effects are considered as an indication B and P atoms were present inside the Si-ncs. However, no evidence of free carrier appearance has been observed. The fact is explained by an essentially increased interaction of carriers with the atom nuclei in Si-ncs.

D/PI.35 THE EFFECT OF ION IMPLANTATION ENERGY AND DOSAGE ON THE MICROSTRUCTURE AND LUMINESCEBCE PROPERTIES OF THE ION BEAM SYNTHESISED FeSi2 IN Si

Y.T. Chong(a,c), C.F. Chow(b,c), N. Ke(b,c), W.Y. Cheung(b,c), S.P. Wong(b,c), K.P. Homewood(d), Q. Li(a,c), (b)Dept. of Physics, The Chinese University of Hong Kong, Hong Kong, China, (b)Dept. of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong, China, (c)Materials Science and Technology Research Centre, The Chinese University of Hong Kong, Hong Kong, China, (d)School of Electronics Engineering, Computer and Mathematics, University of Surrey, Guildford, Surrey GU2 7XH, U.K.

Semiconducting FeSi2 has attracted much attention in the past decade for its potential applications as a silicon-based light emitting material. In this work, FeSi2 precipitates were formed in Si by iron implantation into silicon at low temperature, followed by rapid thermal annealing and furnace annealing. As the luminescence property of the material significantly depends on the fabrication conditions, we carried a systematic study addressing to the two basic fabrication parameters, i.e., the implantation energy and dosage. The structures and light emitting properties of these ion-beam-synthesized FeSi2 precipitates were studied in details using various characterization techniques, including transmission electron microscopy (TEM), Rutherford backscattering spectrometry, x-ray diffraction, and photoluminescence measurements.An interesting evolution of the FeSi2 phase composition has been observed as the two deposition parameters change independently. Both the implantation energy and ion dosage not only affect the morphology and the phase composition of the FeSi2 precipitates, but also the Si matrix (in terms of defects generation) around the precipitates. These are consistent with the experimental observation of the samples' microstructures and their luminescence properties. This work is partially supported by the Research Grants Council of Hong Kong SAR (reference number: CUHK4231/03E).

D/PI.36 ELECTROLUMINESCENCE FROM Si:S LEDS

S.F. Galata, M.A. Lourenço, R.M. Gwilliiam and K.P. Homewood, Advanced Technology Insitute, School of Electronics and Physical Sciences, University of Surrey, Guildford, Surrey GU2 7XH, U.K.

In this study we report light emission from a sulphur related impurity in silicon. Although, sulphur related luminescence from silicon has been reported since the 1980’s, no room temperature luminescence has been achieved and no devices that can be integrated using standard silicon technology have been demonstrated.

Electroluminescence experiments were made on a set of samples of varying sulphur dose and annealing conditions and subsequently implanted with boron to form a pn junction and to introduce dislocation loops. We see two major peaks, at 1129.5 nm which is due to the Si TO phonon assisted transition and at 1363 nm which is due to sulphur related impurities. Sulphur related emission was seen at room temperature in all the samples containing dislocation loop barriers. A model explaining the non-linear EL power dependence is described which shows that there are two major radiative routes via the silicon and the sulphur competing with each other along with a non-

radiative route from the sulphur-related level. The activation energy related to the sulphur level was calculated to be 32±1.5 meV.

D/PI.37 A ROOM-TEMPERATURE OPERATING Si-BASED QUANTUM-DOT LED

M. Jo(a), N. Yasuhara(a), Y. Sugawara (b), and K. Kawamoto(a), and S. Fukatsu(a,c), (a)Graduate School of Arts and Sciences, The University of Tokyo, Komaba, Meguro, Tokyo 153-8902, Japan, (b)JST, Kawaguchi, Saitama 332-0012, Japan, (c)PRESTO, JST, Kawaguchi, Saitama 332-0012, Japan

We report a Si-based light emitting diode (LED) containg GaSb-quantum-dot (QD)-embedded-Si in the active region operating at room temperature. Samples were grown by molecular beam epitaxy on a p-type Si(001). Surface segregation of Sb during growth allows a p-n junction without intentional doping. There is only one active layer that contains a 10-monolayers equivalent of strained GaSb QDs embedded in Si.

EL chips exhibited a good rectifying behavior. The QD EL dominated the spectra at small injection currents whereas the spectral dominance switched to Si at increased current as the QD EL showed a clear saturation trend. A long decay lifetime of 21us was observed in EL decay. These show that the QD EL is not severely affected by dissipative pathways unlike such QD systems as Ge/Si. A low external Q.E. of 0.01% at RT as opposed to 1% at 5K is hence traced back to dissipation of carriers within the Si barriers. This means a higher Q.E. is promised in a stacked QD. Direct modulation of the QD LED was attempted using a 50MHz pulse generator. A fairly fast but truly instrument-limited 3dB roll-off/up time of 6 ns was under a dc bias. The increased bandwidth is accounted for by detrapping of otherwise interface-localized electrons. In view of EL decay under dc bias, a realistic operation bandwidth should lie in the GHz range. On the other hand, we observed a sharp line luminescence feature localized at 900-meV in an post-growth-annealed QD sample. The 900meV line is attributed to (311) defects which develop during annealing as the GaSb/Si QD is a highly strained system and is prone to defect generation to a greater extent. Interestingly, the defect-originated 900-meV line survived up to RT and showed a remarkably nonlinearity in the excitation dependence.

D/PI.38 b-FeSi2-BASED METAL-INSULATOR-SEMICONDUCTOR DEVICES FORMED BY SPUTTERING FOR OPTOELECTRONIC APPLICATIONS

T. Ootsuka(a,b), Z.X Liu(a,b), M. Osamura(a), Y. Fukuzawa(c), N. Otogawa(c), Y. Nakayama(c), H. Tanoue(d), Y. Makita(b,d), (a)System Engineers Co. Ltd., 16-1 Onogawa, Tsukuba 305-8569, Japan, (b)Tateyama Kagaku Industry Co. Ltd., Tsukuba Lab., 16-1 Onogawa, Tsukuba 305-8569, Japan, (c)Kankyo Semiconductors Co. Ltd., 1-1-1 Umezono, Tsukuba 305-8568, Japan, (d)National Institute of Advanced Industrial Science and Technology (AIST), AIST Tsukuba Central 2, 1-1-1 Umezono, Tsukuba 305-8568, Japan

In recent years, semiconductor iron disilicide (b-FeSi2) thin film has attracted extensive research interests owing to its potential applicability for new optoelectronic devices of light emitting diode (LED) and optical sensor both operating at wavelength of ~ 1.5 mm relevant to the quartz optical fiber telecommunication. But, most of the devices up to now were b-FeSi2 / Si heterojunction structures that suffer from the iron diffusion into silicon near the interface during b-FeSi2 formation.

In this work, we fabricated b-FeSi2 films-based metal-insulator-semiconductor (MIS) devices to avoid influences of diffused iron in Si and at the same time to testify the ability of b-FeSi2 thin film as a promising optoelectronic material. b-FeSi2 films were prepared on Si(111) substrates using sputtering. MIS structures were fabricated by depositing a thin SiO2 layer (thinner than 10 nm) and then an aluminum film on SiO2 layer, in which Si was only used as the base for b-FeSi2 epitaxial growth. I-V measurements showed clear rectifying features. Obvious photo-response peaked at a wavelength around 1.46 mm was obtained from the devices having SiO2 layer of about 2.5~10 nm. These results pave the way to the possible realization of a new b-FeSi2 optical sensor operating at 1.5 mm.

D/PI.39 III-V LASERS ON Si: NUCLEATION OF DEFECT-FREE, MONOLITHIC AlSb on Si USING SELF-ASSEMBLED QUANTUM DOTS

D. Huffaker, G. Balakrishnana, L.R. Dawson, C.P. Hains, Y.C. Xin and D.L. Huffaker

We discuss our recent demonstration of photopumped III-V lasers on Si. The room temperature lasing spectrum is centered at 2.0 ºm. The InGaSb quantum well active region is grown atop a defect-free AlSb bulk material on a Si (001) substrate. The highly mismatched epitaxial growth of AlSb on Si is enabled by a monolithic self-assembled AlSb quantum dot (QD) nucleation layer. During the first few monolayers of AlSb growth on Si (001), highly crystalline QDs form. With continued deposition, the islands coalesce into a planar material with no detectable defects. The quality of the buffers is determined by HR-TEM and HR-XRD. The TEM data indicates a defect free AlSb bulk and highly crystalline interface between the Si and the AlSb. The QD nucleation layer facilitates a completely relaxed AlSb within ~100 ML of deposition according to X-Ray diffraction. We attribute the unique growth mode of AlSb on Si to both the large AlSb/Si lattice mismatch (îao/ao=13.5%) in combination with the strong AlSb atomic bond. Materials characteristics and initial device measurements will be discussed.

D/PI.40 THE ELECTRON FIELD EMISSION PROPERTIES OF ION BEAM SYNTHESISED METAL-DIELECTRIC NANOCOMPOSITE LAYERS ON SILICON SUBSTRATES

W.M. Tsang, B. J. Sealy and S.R.P. Silva, Advanced Technology Institute, School of Electronics and Physical Sciences, University of Surrey, GU2 7XH, U.K., S.P. Wong, Department of Electronic Engineering & Materials Science and Technology Research Centre, The Chinese University of Hong Kong, Hong Kong, China

Recently, it has been reported that good electron field emission (FE) properties with turn-on fields as low as 10 V/um can be achieved from ion beam synthesized W-SiC nanocomposite layers due to their electrical inhomogeneity [1]. In the present work, SiO2-Ag nanocomposite layers are synthesised by silver implantation into a silicon dioxide layer, which was grown on a n-type silicon substrate by thermal oxidation, using a high current implanter. The FE properties are studied and correlated with results using other characterisation techniques including atomic force microscopy, Rutherford backscattering spectroscopy, X-ray diffraction, X-ray photoelectron spectroscopy, transmission electron microscopy and ultraviolet photoemission spectroscopy. It is clearly demonstrated that the implanted Ag ions exist in a pure metallic state within the SiO2 matrix. The diameter of the Ag clusters is varied from 8 to 15 nm and depends on the dose of Ag. The FE properties of these samples are found to be dependent on the size of the Ag clusters and these dependencies are discussed with local field enhancement effects due to electrical inhomogeneity. The samples with appropriate Ag doses can give emission currents with electric fields as low as 13 V/um and exhibit a local field enhancement (beta) larger than 300.

1. W.M. Tsang, S.P. Wong and J.K.N. Lindner, "Effect of Tungsten Implantation on the Field Emission Properties of Ion-Beam-Synthesized SiC/Si Layers", Applied Physics Letters, Vol 84, No. 16 3193-3195 (2004).

D/PI.41 THE EFFECT OF PLASMA TREATMENT ON THE PROPERTIES OF GERMANIUM IMPLANTED METAL OXIDE SEMICONDUCTOR STRUCTURES

A.N. Nazarov, Ja.N. Vovk, I.N. Osiyuk, A.S. Tkachenko, I.P. Tyagulskii, V.S. Lysenko, Institute of Semiconductor Physics, National Academy of Sciences of Ukraine, Prospekt Nauki 45, 03028 Kyiv, Ukraine, W. Skorupa, R.A. Yankov, Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf e.V., POB 510119, 01314 Dresden, Germany, T. Gebel, L. Rebohle, Nanoparc GmbH, Bautzner Landstrasse 45, 01454 Dresden, Germany

In the work we used the method of low temperature hydrogen plasma treatment (PT) to increase of the operation time of the Ge-implanted MOS light-emitting diode (MOSLED) without degradation of electroluminescence (EL) intensity in violet range of the spectra.

EL measurements were performed as a function of EL emission wavelength. Additionally, the dependence of the EL intensity at 390 nm on both the applied electric power and the time of electron injection was studied. The values of the constant current voltage applied across the MOSLED structure during EL measurements were also recorded that allows to perform charge trapping calculation. This work has demonstrated the beneficial effects of an optimized plasma treatment on the overall quality of Ge-implanted MOSLEDs. First, such a treatment enables one to achieve an almost four-fold increase in the total injected electron charge just before breakdown, which in turn results in an improvement of the device lifetime. Second, treating MOSLEDs in a plasma discharge containing chemically reactive species like nitrogen and hydrogen leads to appreciable restoration of the oxide matrix. Third, the plasma treatment causes a reduction in the capture cross section of some traps that are responsible for the accumulation of detrimental charges in the oxide, while maintaining unchanged the number of those defect complexes that give rise to the violet EL. Ultimately, the observed improvement of the MOSLEDs' quality is due to the partial removal of specific charge traps, defect passivation, recovery of the oxide network resulting from a relief of internal mechanical stresses, and bond rearrangement. The nature of the plasma interaction with the defect structure of implanted dioxide is discussed.

D/PI.42 SILICON MICROCAVITY LIGHT EMITTING DIODES WITH BURIED COBALT SILICIDE METALLIC MIRRORS

J. Potfajova(a), J.M. Sun(a), T. Dekorsy(a), W. Skorupa(a), B. Schmidt(a), M. Wiemer(b) and M. Helm(a), (a)Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf, P.O. Box 510119, 01314 Dresden , Germany, (b)Fraunhofer Institut f. Zuverlässigkeit u. Mikrointegration, 09126 Chemnitz, Germany

Planar silicon light emitting diodes have only small light output coupling (~5 %) due to the high refractive index of silicon. In order to improve the output efficiency, microcavity light emitting diodes were fabricated with the wafer bonding technology. The silicon microcavity consists of a one-lambda cavity with a buried cobalt silicide metallic mirror and top Si/SiO2 quarter wavelength Bragg mirrors. Room-temperature band-edge electroluminescence (EL) from the microcavity diode was detected under forward injection. The EL spectra show a significant spectral narrowing and an increase of the light output coupling at the cavity mode. The dependence of the electroluminescence on the change of the reflectivity of the top Si/SiO2 Bragg mirrors was studied experimentally. Optimum cavity parameters for efficient output coupling were determined and the results are consistent with the theoretical calculations.

D/PI.43 PHOTOLUMINESCENT SI NANOPARTICLES EMBEDDED IN SILICON OXIDE MATRIX

V. Kapaklis and C. Politis, School of Engineering, Engineering Science Department, University of Patras, 26500 Patras, Greece, P. Poulopoulos, School of Natural Sciences, Materials Science Department, University of Patras, 26504 Patras, Greece, P. Schweiss, Forschungszentrum Karlsruhe, Institut für Festkörperphysik, P.O. Box 3640, 76021 Karlsruhe, Germany

Annealing of bulk SiO at temperatures above 850 C leads to the formation of Si nanocrystals embedded in an amorphous silicon oxide matrix. Structure investigations by X-ray diffraction and transmission electron microscopy reveal a broad size distribution with a large abundance of isolated Si nanocrystals below 5 nm. Strong photoluminescence emission spectra in the near-infrared region were recorded at room temperature and at 100 K with three main emission bands observed. Higher annealing temperatures resulted in increased emission intensities with out significant changes in the spectral shape of the photoluminescence emission. This method could be a promising way to produce Si based photoluminescent materials in large quantities.

D/PI.44 STRUCTURAL AND OPTICAL STUDY OF Ge/Si QUANTUM DOTS ON SI(001) SURFACE COVERED WITH A THIN SILICON OXIDE LAYER

A. Fonseca, E. Alves, Instituto Tecnológico e Nuclear, E.N. 10, 2686-953 Sacavém, Portugal, J.P. Leitão, N.A. Sobolev, M.C. Carmo, Departamento de Física, Universidade de Aveiro, 3810-193 Aveiro, Portugal, A.I. Nikiforov, Institute of Semiconductor Physics, 630090 Novosibirsk, Russia

The growth of extremely high densities (~1012 cm-2) of small-size Ge islands (less than 10 nm) on Si is possible using a thin interlayer of SiO2. Ge layers with a thickness of 0.3, 0.6 or 0.9 nm were deposited on a Si (001) surface covered by a 0.5, 0.75 or 1 monolayer thick SiO2 layer by molecular beam epitaxy at 500°C.

Orientation-dependent Rutherford backscattering measurements were performed enabling the evaluation of the strain in the films using channeling curves taken along the main crystallographic directions. The results suggest a perfect Ge incorporation in the Si lattice for the 0.3 nm thick Ge layer, thus excluding the formation of quantum dots (QDs). For samples with deposition of 0.6 or 0.9 nm of Ge a disturbance of the crystal was detected suggesting formation of strained Ge nanoislands. For the samples with a 0.9-nm-Ge layer a narrowing and a broadening of the experimental curves were observed for the <100> and the <110> directions, respectively. We also made photoluminescence measurements on the as-grown and hydrogen passivated samples. The presence of structural defects was identified. The spectra for the samples with the thicker Ge and silicon oxide layers suggest the presence of QDs.

D/PI.45 Ge SELF-ASSEMBLED ISLANDS GROWN ON SiGe/Si(001) RELAXED BUFFER LAYERS

Z.F. Krasilnik, D.N. Lobanov, A.V. Novikov, M.V. Shaleev, A.N. Yablonsky, Institute for Physics of Microstructures RAS, 603950 Nizhny Novgorod GSP-105, Russia

One possible reason for low intensity of optical recombination in GeSi/Si(001) heterostructures with self-assembled islands at wavelengths 1.3 ? 2 ?m is a weak electron localization near the islands. This problem can be solved by embedding islands in a Si strained layer forming on a GeSi relaxed buffer layer. Here we study the growth and photoluminescence (PL) of Ge islands grown on GeSi/Si(001) relaxed buffer layers.

Relaxed GexSi1-x (x ~ 25 %) buffer layers have been produced using CVD epitaxy and chemical mechanical polishing. Structures with Ge islands on buffer layers were grown by MBE. It was found out that a change in the shape of islands dominating on surface (transition from ?dome? nanoislands to ?hut? clusters) in the case of growth on GeSi buffer layers occurs at higher temperatures than in island growth on Si substrates. Thus, in the case of island growth on GeSi buffer layers we can obtain an array of small hut clusters (quantum dots) at higher

growth temperatures. In the PL spectra of structures with Ge islands built in strained Si layer, besides the dislocation PL lines there is a wide PL peak in the range of wavelengths 1.55 ? 2 ?m, associated with the spatially indirect optical transition between holes in islands and electrons in the Si strained layer.

D/PI.46 PHASE TRANSITION AND LUMINESCENCE PROPERTIES FROM VAPOR ETCHED SILICON

S. Aouida, M. Saadoun, K. Ben Saad, B. Bessaïs

In this work, we propose to present the structure and photoluminescence (PL) properties, under different excitation sources, of a white powder-like ammonium hexafluorosilicate (NH4)2SiF6) obtained from HF/HNO3 chemical vapor etching (CVE) of silicon wafers [1]. The CVE method leads either to the formation of luminescent Porous Silicon (PS) or to the (NH4)2SiF6) depending on the experimental conditions. It was found that the CVE technique can generate, at specific conditions (i.e., HF/HNO3 volume ratio > 1/4), the (NH4)2SiF6 phase instead of PS. The (NH4)2SiF6 marketed powder is not luminescent, while that obtained from silicon vapor-etching presents a noticeable intense and stable photoluminescence (PL) having two shoulders. Two processes have been proposed to explain this PL property. First, the powder was found to contain silicon nanoparticles, which contribute efficiently to visible luminescence at the low energy side. Second, the formation of SiOx features around the silicon nanoparticles lead to oxide related states that may trap electrons or excitons, depending on the silicon nanopraticle size [2], from which radiative recombination leads to a specific PL shoulder at higher energy.

[1] M. Saadoun, N. Mliki, H. Kaabi, K. Daoudi, B. Bessaïs, H. Ezzaouia, R. Bennaceur, Thin Solid Films 405 (2002) 340. [2] M. V. Wolkin, J. Jorne, P. M. Fauchet, G. Allan, C. Delerue, Phys. Rev. Lett.82 (1999) 197.

D/PI.47 DISTRIBUTION OF Ge NANO-ISLANDS ON A SUBSTRATE OF Si UNDER ION BOMBARDMENT

F. Djurabekova, S. Tadjimuratov, Kh. Ashurov, Institute of Electronics, Uzbek Academy of Science, F. Khodjaev str. 33, 700125 Tashkent, Uzbekistan

Ion bombardment is known to make it possible creation of additional nucleation centers in the course of epitaxial growth. In this paper the distribution of nucleus by size in epitaxy process with participation of ions generated under electronic-beam evaporation has been considered. Effect of the ion current density on formation of islands with the same size is studied. Also investigated dependence of the defects formation intensity on the energy of incident ions. Calculations were performed for the cases when Si target undergoes bombarding by Si+ and Ge+ ions. The computations are based on the Monte-Carlo dynamical CASWIN-D code. In this code the motion of ions and knock-on atoms in a target is considered in the framework of pair collision approximation with employment of potentials of Ziegler-Biersack-Littmark (ZBL) and “Kr-C”. The results have been obtained for the energy range from 100 eV up to 1000 eV.

D/PI.48 LUMINESCENT PROPERTIES OF NANOCERAMICS SiO2

V.S. Kortov, A.F. Zatsepin, S.V. Gorbunov, Ural State Technical University-UPI, Department of Physics and Technology, Ekaterinburg, Russia

The study of time-resolved spectra and decay kinetics for cathodo- and photoluminescence of nanoporous ceramics SiO2 induced by electron beam and synchrotron radiation are submitted. Samples under investigation were nanoporous ceramics SiO2 received by a thermal decomposition method of polysilazane (HxCyNzSi) on air at T = 600 °C. It is revealed that the luminescence spectrum of nanoporous SiO2 contains the basic bands with maxima at 2.7, 3.1 and 4.1 eV that are characterized by fast decay kinetics (7ns). The samples annealing on air at T = 1000°C and 1400°C leads to the luminescence spectra transformation induced by thermally reconstruction of defect structure. The spectral shift of luminescence bands and increasing of decay times are found. It is shown that the conversion of electronic structure takes place for various types of the oxygen-deficient centers (ODCs). One of such types ODCs in nanoporous ceramics are silicon clusters (SiSiSi). The neutral oxygen monovacancy (SiSi) being typical ODC-defect in bulk silica are formed as a result of transition from nanoporous amorphous samples to partial-crystalline SiO2 due to a heat treatment in oxidizing atmosphere.

D/PI.49 THE INTENSITY OF THE PL EMISSION AT 0.767 eV AS A FUNCTION OF THE NATURE AND CONCENTRATION OF THERMAL DOUBLE DONORS IN Si

B.A. Andreev, D.I. Kryzhkov, A.N. Yablonskiy, Institute for Physics of Microstructures RAS, GSP-105, 603950 Nizhny Novgorod, Russia and V.V. Emtsev, A.F. Ioffe Physico-Technical Institute, 194021 St.Petersburg, Russia

The origin and emission features of the light emitting centers in Si are of significant interest for the Si-based optoelectronics. P line (0.767 eV) can be observed in the PL spectra of the Si samples annealed at ? ~ 450º?. The formation conditions of the centers, corresponding to the P line are identical to the ones for the thermal double donors (TDD). By the present time, no strong evidence of the connection between the P line and the TDD have been obtained. To clarify this connection we have studied the intensity of the P line as a function of the TDD(1-5) concentration. Strictly linear dependence for the Si samples, annealed under the normal pressure, evidences that the TDD are involved in the process of the radiative relaxation with the energy of 0.767 eV. For the silicon, annealed under the pressure of ~ 1 GPa, the line of the same shape, though with a very different dependence on the TDD concentration has been observed. These facts contradict the statement [1] that the P line corresponds to the transition from the donor level TDD0 with energy Ec-70 meV to a deep acceptor level. To explain the obtained results we assume that the thermal donors are involved only in the process of the energy transfer to the defect centers, corresponding to the P line.

The work was partly supported by INTAS (01-0194 and 03-51-6486), RFBR (04-02-08240 and 05-02-16762). [1] S. Pizzini et al.//J.Phys.:Condens. Matter (2000), 12, p.10131.

D/PI.50 MODELISATION OF OPTOELECTRONIC DEVICE BASED ON Si/SiO2 AND EMITTING A RED LIGHT

N.Sfina, S. Abdi-Ben Nasrallah, A.Bouazra and M. Said Unité de Recherche de Physique des Solides, Département de Physique, Faculté des Sciences de Monastir, 5019 Monastir, Tunisia

In the attempt to realize quantum devices based on a resonant tunneling effect through Si/SiO2 and emitting a red light at a key 0.644 mm wavelength, we have modeled SiO2/Si/SiO2 double barriers embedded between two n-doped Si layers. To study the quantum confinement in Si QW and obtain the potential shape, we have solved a set of coupled Schrodinger-Poisson equations self-consistently. The effects of Si well thickness on quantum confinment of electrons and heavy-holes levels are presented. The energy transition and the overlap integral wave functions between electrons and heavy holes are also examined as a function of well width. The desired red light at a key 0.644 mm wavelength is obtained with an acceptable recombination efficiency given by transition oscillator strength.

D/PI.51 ELECTRIC FIELD EFFECT ON THE SPATIALLY SEPARATED ELECTRON-HEAVY HOLE RECOMBINATION IN Si/SiGe TYPE II QUANTUM WELLS HETEROSTRUCTURES

N. Sfina(a), J.-L. Lazzari(b), S. Abdi-Ben Nasrallah(a) and M. Said(a), (a)Unité de Recherche de Physique des Solides, Département de Physique, Faculté des Sciences de Monastir, 5019 Monastir, Tunisia, (b)Centre de Recherche en Matière Condensée et Nanosciences, CRMC-N, UPR-CNRS 7251 (Laboratoire associé aux Universités Aix-Marseille II et III), Campus de Luminy, Case 913, 13288 Marseille cedex 9, France

We report on optoelectronic properties of devices based on Si/Si1-xGex systems. To limit the inherent problems of the type II character and the indirect nature of the bandgap, we propose Si/Si1-xGex and Si1-xGex/Si strained QWs embedded in relaxed Si1-yGey barriers. The conduction and the valence band present a W-, Usami- or M-like potential profile with a quasi-type I heterostructure. Based on a coupled Schrödinger-Poisson equations, the thickness and compositions (x>y) of these heterostructures are computed in order to get (i) the optimum quantum confinement of electrons and heavy-holes levels, (ii) the optimum out of plane oscillator strength and wave functions overlap (iii) to satisfy a fundamental emission at a key 1.55 mm wavelength below the absorption gap of the three designed structures. The effect of an applied electric field on quantum levels and oscillator strength will be discussed.

D/PI.52 ELECTRICAL PROPERTIES OF B AND Ga Co-DOPED Si

L. Romano, A.M. Piro, M.G. Grimaldi, MATIS - INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, Italy, G. Bisognin, A. Carnera, MATIS - INFM and Dipartimento di Fisica, Università di Padova, Via Marzolo 8, 35131 Padova, Italy

Recent papers reported on the possibility of dopant solubility enhancement due to strain engineering of the Si lattice, while carrier mobility increases in tensile strained Si, these suggestions appears very fascinating for the p-type Si. The Si lattice can be locally strained by doping with substitutional impurities that have different covalent radius with respect of Si: B and Ga.

We will present the electrical performances of Si layers doped with B and Ga in the high concentration regime (>1e20 cm-3). B and Ga have been implanted in order to obtain overlapped profiles into a Si layer previously amorphized by Si implantation. Thermal treatments (580°C-900°C) have been used to recover the crystalline quality by Solid Phase Epitaxy and to activate the implanted dopants. The carrier concentration and mobility have been measured by Hall effect technique. The dopant lattice location and strain profiles have been determined by RBS-channeling. The carrier concentration always coincided with the substitutional dopant concentration and full activation up to a concentration of 3.5e20 and 1.8e20 at/cm3 was detected for B and Ga, respectively, regardless of co-doping. The carrier mobility for B doped samples was definitely higher with respect to Ga. A 50% mobility enhancement in Ga implanted samples with respect to pure Ga implantation occurred upon co-doping with B. The strain in co-doped layer was measured by High Resolution X-Ray Diffraction. At the B and Ga concentration used in this experiment the compressive strain due to Ga was totally compensated by B and, as the average, the co-doped layer was tensile strained. The mobility enhancement in co-doped samples has been interpreted an evidence of a higher carrier mobility in tensile strained Si.

Wednesday, June 1, 2005 **Afternoon**
Mercredi 1er juin 2005 Après-midi

Session V : SiGe-based materials
Session chair: B. Ghyselen

D-V.01 14:00 -Invited-

ENGINEERED SUBSTRATES AND THEIR FUTURE ROLE IN MICROELECTRONICS
Eugene A. Fitzgerald, MIT, Dept. of Materials Science and Engineering, Cambridge MA, USA

D-V.02 14:30

HIGH GERMANIUM CONTENT SIGE VIRTUAL SUBSTRATES GROWN AT HIGH TEMPERATURES
Y. Bogumilowicz(a), J.M. Hartmann(b), F. Laugier(b), G. Rolland(b), T. Billon(b), N. Cherkashin(c) and A. Claverie(c), (a)STMicroelectronics, 850 rue Jean Monnet, 38921 Crolles Cedex, France, (b)CEA-DRT, LETI / D2NT & DPTS, CEA – GRE, 17 avenue des Martyrs, 38054 Grenoble Cedex, France, (c)nMAT Group, CEMES/CNRS, BP 4347, 31055 Toulouse Cedex, France
We have grown SiGe virtual substrates in Reduced Pressure - Chemical Vapour Deposition. We have focused on the effects of both the growth temperature and the final Ge concentration on their structural properties. For Si0.8Ge0.2 virtual substrates, the macroscopic degree of strain relaxation increases (95% to 97%) when the growth temperature increases (750 to 950°C). Increasing the growth temperature has no real effect on the surface rms roughness of Si0.8Ge0.2 virtual substrates (in-between 2 and 3 nm), whereas it drastically decreases the density of both field and pile-up threading dislocations densities (TDD) (from 1E6 down to 1E5 cm-2 for field TDD, and from 1E6 to 1E4 cm-2 for pile-up TDD). Therefore, high growth temperatures are clearly advised to obtain good structural properties.
When increasing the Ge concentration of virtual substrates grown at 850°C or 900°C from 20% up to 50%, the macroscopic degree of strain relaxation increases from 96% up to more than 100% (i.e. from a compressive residual strain to a tensile one). The surface rms roughness increases as well as the Ge concentration increases, more strongly for a growth temperature of 900°C than 850°C (max rms = 81 nm at 900°C). This increase of the surface roughness has little impact on the field TDD (4x1E5 cm-2 at 850°C and 2x1E5 cm-2 at 900°C) whereas it increases the density of pile-up threading dislocations (from slightly more than 1E4 up to 2x1E5 cm-2). Dual channel heterostructures made of a tensile strained silicon channel on top of a compressive strained Ge channel itself on top of a SiGe 50% virtual substrate have been obtained using optimized growth conditions. Short term perspectives are the development of SiGe virtual substrates with Ge content above 50%.

D-V.03 14:45

INVESTIGATION OF HYDROGEN IMPLANTATION INDUCED BLISTERING IN SiGe
R. Singh, I. Radu, M. Reiche, R. Scholz, U. Gösele, and S. H. Christiansen, Max Planck Institute of Microstructure Physics, Weinberg 2, 06120, Halle/Saale, Germany, D. Webb, International Rectifier Epi Services Inc., 550 W. Juanita Ave, Mesa AZ 85210, USA
Strain-relaxed Si0.78Ge0.22 layer (~4 µm thick) was grown on an 8-inch Si(001) substrate by reduced pressure chemical vapour deposition which serves as virtual substrate for the epitaxial growth of ultrathin biaxially, tensile strained silicon. When this wafer is implanted with hydrogen ions (H2+ at 240 keV with dose of 5´1016 cm-2), bonded to an oxidized Si(001) handle wafer and subsequently annealed at elevated temperatures (>400°C) for a sufficiently long time, strained silicon-on-insulator (sSOI) can be obtained when the transferred Si0.78Ge0.22 layer is selectively etched away. For the fabrication of sSOI it is very important to understand the physical mechanisms and kinetics of the blistering (single wafer) or exfoliation (bonded wafer) based on hydrogen agglomeration during annealing. Our present investigation focuses on the blistering in implanted Si0.78Ge0.22 layers during annealing at temperatures ranging from 300-700°C. The surface topography of the blisters was determined using optical microscopy in Nomarski mode, atomic force microscopy and stylus profilometry. The characterization of hydrogen implantation induced damage and defects inside Si0.78Ge0.22 layer was done using cross-sectional transmission electron microscopy. The Arrhenius plot of blistering time versus annealing temperature reveals two different activation energies of blistering. In the low temperature regime (300-400°C), an activation energy of 1.2 eV is obtained while in the high temperature regime (400-700°C), the activation energy is 0.38 eV. Based upon this blistering study, an appropriate annealing temperature and time was chosen for the layer splitting in Si0.78Ge0.22 which was implanted with hydrogen and bonded to an oxidized Si(001) handle wafer which ultimately yields sSOI wafer.

D-V.04 15:00

STRAIN CHARACTERIZATION IN STRAINED-Si MOSFET CHANNELS BY NBD METHOD

K. Usuda, T. Numata, T. Irisawa, N. Hirashita and S. Takagi(a,b), MIRAI-ASET, (a)MIRAI-ASRC/AIST, (b)The University of Tokyo, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan

A strained-Si MOSFET is an attractive device structure for advanced high-performance CMOS. When fabricating this device, an integration technique for controlling strain in strained-Si channels is indispensable. However, the strain variation in the channel has not been investigated in detail, because a very small probe realizing direct observation in the channel is not yet available. This paper presents a successful strain evaluation in the strained-Si MOSFET channels with short gate length. In order to evaluate the local strain in the channel, we have developed a new method with high spatial resolution using nano-beam electron diffraction (NBD) [1]. The lateral spatial resolution and the lattice spacing measurement precision in this method were 10 nm and within ±0.1%, respectively. Strained-SOI MOSFETs with gate length of Lg=35nm, fabricated on SGOI substrates, were used for strain evaluation. As a result, NBD has clearly shown that tensile strain along the strained-Si channel after the device fabrication process. Furthermore, it was revealed that the strain was uniform inside the channel and maintained even at the channel edge regions. In conclusion, the NBD method is well suited for evaluating strain variations within such extremely thin and short channels. This work was supported by NEDO.

[1] K.Usuda et al., Appl. Surf. Sci., Vol.224, p.113 (2004)

D-V.05 15:15

IMPROVED HOLE MOBILITIES AND THERMAL STABILITY IN A STRAINED-Si/STRAINED-Si1-yGey/STRAINED-Si HETEROSTRUCTURE GROWN ON A RELAXED Si1-xGex BUFFER

Saurabh Gupta, Minjoo L. Lee, David M. Isaacson and Eugene A. Fitzgerald, Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge MA 02139, USA

A dual channel heterostructure consisting of strained-Si/strained-Si1-yGey on a relaxed Si1-xGex buffer (y>x), provides a platform with high hole mobilities (μeff) that depend directly on y in the Si1-yGey layer. Ge out-diffusion from the strained-Si1-yGey layer into the relaxed Si1-xGex buffer, which occurs during high temperature processing, reduces the peak Ge concentration in the strained-Si1-yGey layer and degrades hole μeff in these dual channel heterostructures.

We present a tri-layer heterostructure of strained-Si/strained-Si1-yGey/strained-Si grown on a relaxed Si1-xGex buffer. The Ge diffusion coefficient in tensilely strained Si is very low, leading to much reduced Ge out-diffusion from the strained-Si1-yGey layer in the tri-layer heterostructure. Numerical investigations and SIMS results establish that tri-layer heterostructures retain a higher peak Ge concentration in the strained-Si1-yGey layer than corresponding dual channel heterostructures after identical thermal treatment. Ring shaped MOSFETs were fabricated on both platforms and subjected to varying processing temperature in order to compare the extent of μeff reduction with thermal budget. Hole μeff enhancements are retained to a much higher extent in a tri-layer heterostructure after high temperature processing as compared to a dual channel heterostructure. The improved thermal stability of a tri-layer heterostructure combined with improved hole μeff provides a platform for fabricating high μeff p-MOSFETs which can be processed over higher temperatures without significant losses in hole μeff.

D-V.06 15:30

MOBILITY-LIMITING MECHANISMS IN SINGLE AND DUAL CHANNEL STRAINED Si/SiGe MOSFET'S

S.H. Olsen(a), P. Dobrosz(b), E. Escobedo-Cousin(a), S.J. Bull(b) and A.G. O'Neill(a), (a) School of Electrical, Electronic and Computer Engineering, University of Newcastle, U.K., (b) School of Chemical Engineering and Advanced Materials, University of Newcastle, U.K.

Dual channel strained Si/SiGe CMOS architectures have recently received attention due to maximum performance benefits being predicted for both n- and p-channel MOSFETs. Epitaxial growth of a compressively strained SiGe layer followed by tensile strained Si can create a high mobility buried hole channel and a high mobility surface electron channel on a single relaxed SiGe virtual substrate. However dual channel n-MOSFETs fabricated using a high thermal budget exhibit compromised mobility enhancements compared with single channel devices, in which both electron and hole channels form in strained Si. This paper investigates the mobility-limiting mechanisms of dual channel structures. The first evidence of increased interface roughness due to the introduction of compressively strained SiGe below the tensile strained Si channel is presented. The interface corrugations degrade electron mobility in the strained Si. Roughness measurements have been carried out using AFM, TEM and XRD. Filtering AFM images allowed roughness at wavelengths pertinent to carrier transport to be studied. The results are in agreement with electrical data and suggest that there is a greater impact of surface roughness than Ge out-diffusion (from the high Ge-content buried SiGe layer) on dual channel n-MOSFET performance. Furthermore, the first comparison of strain measurements in the surface channels of single and dual channel architectures is presented. Raman spectroscopy has been used to study channel strain both before and after processing and indicates that there is no impact of the buried SiGe layer on surface macrostrain. The results provide further evidence that the improved performance of the single channel devices fabricated using a high thermal budget arises from improved surface roughness.

15:45 **BREAK**

Session VI : TCAD
Session chair: W. Windl

D-VI.01 16:05 -Invited-

TRENDS, DEMANDS and CHALLENGES IN TCAD

Ingo Bork, Victor Moroz and Dipu Pramanik, Synopsys, USA

Currently TCAD is most heavily used in the device research and process integration phases of a technology cycle. However, a major trend visible in the industry is the demand to apply TCAD tools far beyond the integration phase into manufacturing and yield optimization. Short IC product lifetimes make fast yield ramp-up critical for being profitable and TCAD tools build a bridge between IC design and manufacturing. Another major trend is to use TCAD to estimate layout dependent stress variations and account for these variations in circuit design rules for the layout of standard cells and custom ICs. This talk gives an overview of those trends and addresses resulting challenges for model development and calibration.

D-VI.02 16:35

AMORPHOUS LAYER DEPTH AND RESIDUAL DAMAGE DEPENDENCE ON IMPLANT PARAMETERS DURING Si SELF-IMPLANTATION

Pedro Lopez, Lourdes Pelaz, Luis A. Marques, Juan Barbolla, Dpto. de Electricidad y Electrónica, Universidad de Valladolid, E.T.S.I. Telecomunicación, Campus Miguel Delibes s/n, 47011 Valladolid, Spain, H.-J.L. Gossmann, Aditya Agarwal, Axcelis Technologies, 108 Cherry Hill Drive, Beverly MA 01915, USA, Kenji Kimura, Tomoyoshi Matsushita, Department of Engineering Physics and Mechanics, Kyoto University, Kyoto 606-8501, Japan

Preamorphization followed by low temperature solid phase epitaxial regrowth has been proved to provide a high activation of the dopants with minimal diffusion. However, the end of range damage beyond the initial amorphous-crystalline (a/c) interface, present after regrowth, causes diffusion and deactivation of dopants. Therefore, an accurate prediction of the a/c interface depth, and hence of the quantity and position of end of range damage, is necessary for the adequate control of the carrier concentration. In this work we study the influence of implant conditions on the depth of the amorphous layer and the amount of residual damage during Si self-implantation. We compare experimental data obtained by RBS with our simulation results obtained using an atomistic amorphization-recrystallization model recently developed. We show that the a/c interface depth initially increases with dose but saturates at high doses. Beam current and wafer temperature also alter the depth of the amorphous layer by affecting the dynamic annealing of the damage. Consequently the amount of residual damage is modified, affecting the redistribution of dopants in the regrown layer during subsequent annealing. These parameters are not always well controlled or specified in experiments and can explain differences observed in dopant profiles.

D-VI.03 16:50

OPTIMISED MODEL OF THE EXTENDED DEFECTS APPLIED TO NON-AMORPHISING IMPLANTS

E. Lampin, IEMN-UMR CNRS 8520, Av. Poincaré, 59652 Villeneuve d'Ascq Cedex, France, F. Cristiano, Y. Lamrani, D. Connetable, LAAS/CNRS, 7 Av. du Col. Roche, 31077 Toulouse, France

In this paper, a physical model for the kinetics of extended defects based on an atom-by-atom description of their evolution is optimised and applied to non-amorphising implants. The whole characteristics of the defects from small clusters to \{113\} defects and to dislocation loops is contained in the model. In the first part, the numerics as well as the physics of the model are optimised : the computational time is reduced and the main parameters of the model, i.e. the formation energies of the small clusters, the fault energy of the \{113\} defects and their Burgers vector, are determined using existing and dedicated experiments. In these experiments, small clusters and \{113\} defects form near the surface and dissolve when the annealing goes on.

D-VI.04 17:05

PHYSICALLY-BASED MODELLING OF DISLOCATION LOOPS IN ION IMPLANTATION PROCESSING IN SILICON

P. Castrillo, I. Martin-Bragado, R. Pinacho, M. Jaraiz, J. E. Rubio, K.R.C. Mok, and J. Barbolla, Department of Electronics, University of Valladolid, 47011 Valladolid, Spain

Under certain conditions, particularly for high-dose implants, {311} rod-like defects can evolve into dislocation loops (DLs). The formation of DLs entails a strong decrease of the interstitial supersaturation, drastically affecting dopant diffusion. Then, in order to simulate the final dopant profiles, it is crucial to predict the formation of DLs, as well as their subsequent growth and interaction with dopants. In this work we have explored the capabilities of the atomistic kinetic Monte Carlo (kMC) simulation method to reproduce a wide range of phenomena related to DLs in ion implantation and annealing processes. We take advantage of the ability of this method to incorporate multiple mechanisms and interactions in a detailed yet simple way. DLs are implemented according to realistic geometries, giving a direct assessment of the correct capture volume for diffusing defects. A temperature dependent transition-size model is used for the transformation of {311} defects into DLs. The model has been included and calibrated in a kMC simulator. This simulator provides an excellent description of the size distribution of {311} defects (required for a size-based model) and of the amorphization and recrystallization (needed to provide reliable information on the number of interstitials in the end-of-range region, EOR). The model correctly predicts the presence of DLs in a wide variety of conditions for ion implants and subsequent annealing and allows the accurate simulation of dopant diffusion after amorphizing implants. Boron pile up at the EOR region is also reproduced.

D-VI.05 17:20

ACCURATE AND EFFICIENT TCAD MODEL FOR THE FORMATION AND EVAPORATION OF SMALL INTERSTITIAL CLUSTERS AND {311} DEFECTS IN SILICON

Christoph Zechner, Nikolas Zographos, Dmitri Matveev, Axel Erlebach, Synopsys Schweiz AG, Affolternstr. 52, 8050 Zurich, Switzerland

In recent years physics-based models have been developed for the time evolution of defects formed by Si self-interstitials in ion-implanted Si. However, the most accurate models use too many equations for TCAD applications. We present a new model, in which five reaction equations are sufficient to describe the physics behind interstitial clusters and {311} defects. Three equations are needed to describe the kinetics of small interstitial clusters (I2, I3, I4) which governs the initial phase of implantation damage annealing. Two equations describe the formation and Ostwald ripening of {311} defects.
The model has been implemented in the process simulator FLOOPS and calibrated with a large collection of published SIMS and TEM data for silicon implantation and annealing. It allows efficient, predictive simulations of interstitial cluster kinetics in a wide range of process conditions.

D-VI.06 17:35

A COMPREHENSIVE SOLUTION FOR SIMULATING ULTRA-SHALLOW JUNCTIONS: FROM HIGH DOSE/LOW ENERGY IMPLANT TO DIFFUSION ANNEALING

F. Boucard, F. Roger, I. Chakarov, V. Zhuk, M. Temkin, X. Montagner, E. Guichard, Silvaco Data Systems, 55 rue Blaise Pascal, 38330 Montbonnot, France and D. Mathiot, CNRS Phase, 23 rue du Loess, 67037 Strasbourg, France

The persistent semiconductor technology trend of shrinking down device size requires the development of very aggressive technological setups consisting in high dose/low energy implants, followed by rapid thermal anneals (RTA). Since it is now well established that phenomena involved in ion implantation will play a key role in transient enhanced diffusion (TED), advanced process simulation tools need to model accurately these two steps for deep submicron CMOS technologies. This paper presents a comprehensive solution, fully integrated into the commercial SILVACO TCAD suite, which includes the latest physical model developments needed by advanced process technology designers. Initial impurity and defects profiles generated during the implantation step are analytically described using an original Legendre polynomials approach. For the diffusion model, all interactions between dopant and defects are taken into account accordingly to complex physical phenomena. Eventually a global and original calibration methodology has been used to provide the model with a physical set of parameters which allows to successfully simulate in 1D and 2D a very broad range of advanced experimental setups, from low to high energy and dose implants followed by anneals ranging from a few seconds to tens of minutes.

D-VI.07 17:50

BORON ACTIVATION AND REDISTRIBUTION DURING THERMAL TREATMENTS AFTER SOLID PHASE EPITAXIAL REGROWTH

Maria Aboy, University of Valladolid, Lourdes Pelaz, University of Valladolid, Juan Barbolla, University of Valladolid, R. Duffy, Philips Research Leuven, V.C. Venezia, Axcelis Technologies

Solid phase epitaxial regrowth (SPER) is one of the most promising techniques for achieving acceptable active dopant and junction depth values to meet the performance specifications of the international technology roadmap of semiconductors. Active B concentrations up to a few times 1020 cm-3 are achieved after the low temperature recrystallization process, while higher concentrations are immobilized in B clusters and thus, remain inactive. In this work we analyze the activation and evolution of B profiles during annealing after SPER. Sheet resistance measurements are used to study B activation while SIMS provides the evolution of B profiles. Kinetic Monte Carlo atomistic simulations are compared to experiments providing a good insight into mechanisms that drive these phenomena. Simulations show that the presence of end of range (EOR) defects, still present beyond the amorphous/crystalline interface after regrowth, leads to additional deactivation during subsequent anneal treatments. Moreover, B uphill diffusion towards the surface is observed in the high concentration region, while downhill diffusion occurs in the tail region of the B profile. During prolonged anneals B activation decreases until it reaches a minimum, which is lower for low annealing temperatures. Finally, when EOR defects dissolve or reach very stable configurations such us dislocation loops, B reactivation is observed as well as B tail diffusion, which are controlled by the dissolution of B clusters.

D-VI.08 18:05

IMPACT OF LARGE ANGLE TILT IMPLANTATION ON THE THRESHOLD VOLTAGES OF LDMOS TRANSISTOR ON SOI

H. Xu, E. Lampin, E. Dubois, IEMN, Av. Poincare, 59652 Villeneuve d'Ascq, France

A purely vertical (0°) implantation and a Large-Angle Tilt Implantation called LATID (usually 45°) are generally used to form the short channel for LDMOS transistors. A modeling of both implantations is first extended to include the geometrical effects of the LATID as well as the strong channeling of the vertical implantation. The enhancements are validated by a comparison of the simulated doping profiles and sheet resistances with their experimental values.

In a second step, based on this accurate modeling of channeling, the threshold voltage of an 8 nm-gate-oxide n-LDMOS transistor on SOI is calculated and successfully compared with experience. An optimization is then carried on for a new generation of 7 nm-gate-oxide LDMOS. This transistor suffers a degradation of the threshold voltage because the implantation ions penetrate through the gate oxide and modify the channel conditions such as the length and the concentration peak. The impact of temperature, implantation energy and tilt angle are simulated and the threshold voltage is adjusted by device simulations. It is found that the impact of LATID implantation is important on the channel condition which links directly to the threshold voltage. A 60° tilt with some energy modifications gives very good adjustment. A comparison of the two gate-oxide thicknesses with the optimized channel condition is shown at last.

19:00 **AWARD CEREMONY**

The symposium organizers and the candidates to the graduate student award are requested to attend.

CONFERENCE RECEPTION

Session VII : Dopant characterization
Session chair: D. De Salvador

D-VII.01 9:00 -Invited-

SCANNING SPREADING RESISTANCE MICROSCOPY (SSRM) 2D CARRIER PROFILING FOR ULTRSHALLOW JUNCTION CHARACTERIZATION IN DEEP-SUBMICRON TECHNOLOGIES

Pierre Eyben(a), Tom Janssens(a) and Wilfried Vandervorst(a,b), (a)IMEC vzw, Kapeldreef 75, 3001 Leuven, Belgium, (b)K.U. Leuven, Electrical Engineering Dept., INSYS, Kasteelpark Arenberg 10, 3001 Leuven, Belgium

Experimental and modelling improvements in scanning spreading resistance microscopy (SSRM) as well as the advent of new generations of full diamond moulded probes have put the SSRM technique inline with the stringent ITRS requirements for two-dimensional dopant profiling. At the moment, SSRM is therefore a powerful and unique tool for the analysis of existing technologies and the support in development of new technologies where mechanisms as lateral diffusion, stress induced diffusion or partial activation have an increasing importance.

This work presents the recent progress in SSRM capabilities highlighting simultaneous performances in terms of sensitivity (<10%), spatial resolution (1-3nm), dopant gradient resolution (1-2nm/dec), and quantification accuracy. The latter is demonstrated through the analysis of different carrier profiling applications i.e. the calibration of process simulations for a 90nm n-MOS technology, the determination of the impact of nitridation on the lateral diffusion in a 40nm n-MOS technology and the study of activation and diffusion problems in SPER-anneals of shallow implants, the observation of stress-induced diffusion mechanisms in the vicinity of shallow trench isolations (STI) and the study of diffusion and mobility mechanisms in SiGe MOS structures. Moreover, comparison with STM results demonstrates that with SSRM a similar resolution can be reached with however superior concentration sensitivity and junction position identification as STM presents an inferior signal/noise ratio. Compared to SCM, SSRM provides a spatial resolution which is 10x higher and an unparallel concentration sensitivity and quantification accuracy. For instance none of the HALO-profiles are detectable either with STM nor with SCM.

D-VII.02 9:30 -Invited-

SCM 2D CARRIER PROFILING FOR ULTRASHALLOW JUNCTION CHARACTERISATION IN DEEP-SUBMICRON TECHNOLOGIES

F. Giannazzo, V. Raineri, CNR-IMM, sezione di Catania, Stradale Primosole 50, 95121 Catania, Italy, E. Bruno, S. Mirabella, G. Impellizzeri, F. Priolo, MATIS-INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, Italy, M. Fedele, R. Mucciato, 2M Strumenti, Via G. Pontano 9, 00141 Roma, Italy, E. Napolitani, MATIS-INFM and Dipartimento di Fisica dell'Università di Padova, Via Marzolo 8, 35131 Padova, Italy

We review our recent work on scanning capacitance microscopy as a quantitative carrier profiling method on nanometric profiles. In particular, we address the nanodevice (tip, dielectric and semiconductor) fabrication necessary to obtain quantifiable and reliable measurements. Comparisons among different tips, dielectrics and dielectric/semiconductor interfaces will be shown to demonstrate their importance, how they affect measurements and their influence on quantification. Several concepts in quantification methods used will be considered. Furthermore, the comparison between two different atomic force microscopes, i.e. DI3100 by Veeco and XE-100 by PSIA, equipped with different SCM sensors, will undertake the hardware aspects. The respective components of the error and the final precision of the method is then determined. Furthermore, sensitivity and resolution are also deeply discussed considering measurements on special designed samples containing quantum wells of Si0.75Ge0.25 layers strained between Si films. Quantum wells with different widths down to 1 nm and doped with different B concentrations ranging from 1016 to 1019 cm-3 are considered. Measurements were taken on sample cross-sections and on bevelling. A spatial SCM resolution of 1 nm is demonstrated not only in terms of signal sensitivity, but also in terms of quantitative majority carrier profiling in all the considered concentration range.

Furthermore, we applied the method to image directly submicron devices in Si and high performance power devices on non-conventional materials. Examples of applications in deep-submicron technologies are the study of B diffusion and electrical activation, point defects influence on dopant distribution, size effects in nanostructures.

D-VII.03 10:00

TWO-DIMENSIONAL GEOMETRICAL EFFECTS OF CONFINED B CLUSTERS IN DEEP SUBMICRON STRUCTURES

E. Bruno, S. Mirabella, G. Impellizzeri, F. Priolo, MATIS-INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, Italy, F. Giannazzo, V. Raineri, CNR-IMM, Sezione di Catania, Stradale Primosole 50, 95121 Catania, Italy, E. Napolitani, MATIS-INFM and Dipartimento di Fisica, Università di Padova, Via Marzolo 8, 35131 Padova, Italy

The last decades have been characterized by a continuous scaling down of Si-based electronic device sizes, according to the continuously increasing market requirements. Many scientific and technological efforts have been carried out in this direction, but the confinement of high dopant amounts causes several detrimental phenomena. First of all, the extremely high gradient leads dopants to rapidly diffuse at disadvantage of the junction extension. Moreover, when dopants are present at high concentration, part of them precipitates, losing their electrical activation, also at concentration lower than the solubility limit in c-Si. This commonly occurs after dopant implantation, because of dopant-damage interaction.

We investigated the clustering of B implanted in confined regions in the deep submicron scale, analysing the B active concentration by means of scanning capacitance microscopy. Upon a B multi-delta structure grown by molecular beam epitaxy, we implanted a dose of 2x10^14 B/cm^2 at 3 keV through a previously deposited 600 nm thick mask of SiO2 with submicron openings down to 0.1 µm. We found that, after an annealing at 800°C, the active B concentration increases by one order of magnitude going from 3.2 to 0.1 µm windows width, as well as the junction depth shrinks, both due to the damage reduction produced by the opening decreasing. The cluster dissolution in two-dimensions is also studied by the B re-activation during prolonged annealings. The found geometrical effects have a quite strong implications in modern microelectronics demonstrating for the first time the possibility to increase the B activation in deep submicron devices.

D-VII.04 10:15

NON DESTRUCTIVE CHARACTERIZATION OF USJ FOR NODE 45 nm USING INFRA RED SPECTROSCOPIC ELLIPSOMETRY (IRSE)

J.L. Stehle, Adrien Darragon, Christophe Defranoux, Sopra-SA, 26 rue Pierre Joigneaux, 92270 Bois Colombes, France

The source and drain of next generation node 45 nm must have ultra shallow junction, maybe laser annealed, and the extensions must be measured with sub nm pecision, according to the ITRS 2003. Actual measurement techniques are destructive or based upon elementary analysis (SIMS) which cannot take into account the electrical activity of the annealed layer. This presentation will describe the new IRSE instrument and the USJ application. The fundamental principle of IR and spectroscopic ellipsometry will be explained briefly, and the refined Drude model used for the regression will be emphasised. The technique is a first principle and does not require calibration nor reference material nor reference spectrum. The optical scheme of the tool will be presented and particularly the way to suppress the effect of the back side reflexion interference. Thus the signal becoming pure, the modelling can be applied totally. The spot size reduced to 85 x 200 µm is very keen for edge exclusion and local measurements, even in the scribe line, with pattern recognition. Several applications as thin epis, multiple layers and USJ will be presented. The laser annealed USJ will be compared to SPR and RTP results. The active dopants dose compared to SIMS can give the efficiency of annealing process, the conductivity and mobility are assessed and the depth profile can be measured accurately, so finally the sheet resistance is given for the range of USJ layers. The IRSE is a powerful tool for USJ application with non contact, small spot and fast measurements. Rs, Xj, dose and mobility are extracted together in one measurement. Ref : E-MRS 04, Clarisse Trudeau, IMEC

D-VII.05 10:30

APPLICATION OF THE TOMOGRAPHIC ATOM PROBE TO THE INVESTIGATION OF NANOSCALED MATERIAL DEVICES BY MEANS OF FEMTOSECOND LASER PULSES

P. Pareige(a), H. Bernas(b), F. Vurpillot(a), B. Gault(a), M. Gilbert(a), E. Cadel(a) and B. Deconihout(a), (a)GPM UMR CNRS 6634, Université et INSA de Rouen, 76801 Saint-Etienne du Rouvray Cedex, France, (b)Centre de Spectrométrie Nucléaire et de Spectrométrie de Masse (UMR 8609), CNRS–IN2P3, Université d'Orsay, France

The Scanning Capacitance Microscopy is a widely used method for the characterisation of doping profiles in the structures of the microelectronics industry. Because of it is relatively easy to implement, and because it is able to discriminate between n-type and p-type dopants, SCM has demonstrated its capabitilities to be a valuable tool for device failure check. However, the future devices require a nanometric resolution and precise quantification of the dopant concentration, and SCM still lacks reproducibility and spatial resolution compared to other methods like Scanning Spreading Resistance Microscopy (SSRM).

One of the main problems which hampers the reproducibility of the SCM measurements is the quality of the oxide. We aim in this paper to evaluate the performances of a detection method, the Scanning Schottky Capacitance Microscopy (SSCM), which suppresses the oxide involved in the SCM. Test samples (delta-doped layers and staircases) are used to characterise the spatial resolution, the reproducibility and the capabiblities in terms of quantification of this method.

10:45 **BREAK**

Session VIII : Point defects
Session chair: I. Bork

D-VIII.01 11:05 -Invited-

ATOMISTIC SIMULATIONS IN Si PROCESSING: BRIDGING THE GAP BETWEEN ATOMS AND EXPERIMENTS

Luis A. Marqués, Departamento de Electrónica, E.T.S.I. de Telecomunicación, Universidad de Valladolid, 47011 Valladolid, Spain

With devices shrinking to nanometric scale, process simulation tools have to shift from continuum models to an atomistic description of the material. However, the limited sizes and time scales accessible for detailed atomistic techniques usually lead to the difficult task of relating the information obtained from simulations to experimental data. The solution consists of the use of a hierarchical simulation scheme: more fundamental techniques are employed to extract parameters and models that are then feed into less detailed simulators which allow direct comparison with experiments. This scheme will be illustrated with the modelling of the amorphization and recrystallization of Si, which has been defined as a key challenge in the last edition of the International Technology Roadmap for Semiconductors. The model is based on the bond defect or IV pair, which is used as the building block of the amorphous phase. The properties of this defect have been studied using ab-initio methods and classical molecular dynamics techniques. It is shown that the recombination of this defect depends on the surrounding bond defects, which accounts for the cooperative nature of the amorphization and recrystallization processes. The implementation of this model in a kinetic Monte-Carlo code allows extracting data directly comparable with experiments. This approach provides a physical insight of the amorphization and recrystallization mechanisms and a tool for the optimization of SPE related p

D-VIII.02 11:35

AB-INITIO CALCULATIONS OF THE INTERACTION BETWEEN NATIVE POINT DEFECTS IN SILICON

G. Hobler(a), G. Kresse(b), (a)Inst. f. Festkörperelektronik, Vienna University of Technology, Vienna, Austria, (b)Inst. f. Materialphysik, University of Vienna, Vienna, Austria

Annealing of defects during and after room-temperature ion implantation is known to significantly affect the amount of implantation damage. At not too high defect levels annealing is determined by the competition between I-V recombination and V-V and I-I clustering. Previous studies using BC and kLMC simulations [1,2] have shown that in general the amount of damage is overestimated compared to experiment if similar capture radii are used for I-V, V-V, and I-I reactions. In this work we present ab-initio calculations of the interaction potential between I-V, V-V, and I-I pairs placed at different interatomic separations. Structural relaxation is mostly done in 216-atom supercells. In a few cases 512-atom supercells have been used. The results show much stronger interaction between I and V than between defects of the same kind, thus indicating that I-V recombination is significantly favored compared to vacancy and interstitial clustering.

[1] G. Hobler et al., Nucl. Instr. Meth. B, in press.
[2] G. Otto, D. Kovac, G. Hobler, Nucl. Instr. Meth. B, in press.

D-VIII.03 11:50

DETECTION OF POINT DEFECTS VACANCIES, SELF-INTERSTITIALS AND THEIR COMPLEXES IN SILICON BY ELECTRON ENERGY LOSS SPECTROSCOPY

Gerd Duscher*, Nathan Stoddard, and Wolfgang Windl*, Materials Science and Engineering Department, North Carolina State University, Raleigh NC 27695-7916, USA, * and Condensed Matter Science Division, Oak Ridge National Laboratory, Oak Ridge TN 37831, USA, ** Department of Materials Science and Engineering, The Ohio State University, Columbus OH 43210-1178, USA

Nitrogen doped silicon samples were irradiated with 200 kV electrons in a transmission electron microscope (TEM). The resulting room temperature point defect creation, bonding and segregation were studied by in situ conventional and Z-contrast TEM imaging and electron energy-loss spectroscopy. Energy-loss spectra from areas attributed to be rich in vacancies or silicon self-interstitials are found to be significantly different from the bulk in the near-edge structure of their Si-L2,3 edges. The experimental results are compared with ab initio density of states calculations for electronically excited atoms near relaxed point defect structures of V, V2, V3, I, and I3. This comparison enables us to determine the detection limit of point defects in Si for different electron microscopes.

D-VIII.04 12:05

ION IMPLANTATION AND ELECTRON IRRADIATION DAMAGE IN UNSTRAINED GERMANIUM AND SILICON-GERMANIUM ALLOYS

A.R. Peaker, V.P. Markevich, University of Manchester, Manchester M60 1QD, U.K., L.I. Murin, Institute of Solid State and Semiconductor Physics, Minsk 220072, Belarus, N.V. Abrosimov, Institute of Crystal Growth, Berlin 12489, Germany, V.V. Litvinov, Belarussian State University, Minsk 220050, Belarus

The possibility of making mainstream semiconductor devices which use the high electron and hole mobility of Ge and Ge rich SiGe alloys has drawn attention to the very limited knowledge base regarding ion implantation damage and its removal in germanium. In this paper we present measurements of point defects using DLTS and Laplace DLTS on Ge irradiated with gamma-rays or MeV electrons and the ensuing defect reactions that occur during annealing. This is compared with damage induced by 2 MeV Si implantation into Ge at both low and high doses and its subsequent removal by furnace annealing. Similar experiments have been performed on Ge rich SiGe to study the sitting preferences of defects. The focus of the work has been on vacancy related defects because of their technological importance. It is thought that the diffusion of both acceptors and donors is vacancy mediated in Ge and so vacancy clusters rather than interstitial clusters are expected to be the significant defects in transient enhanced diffusion. Vacancy related defects have been also implicated in limiting the maximum electron concentration in Ge and Ge rich SiGe. These issues will be discussed in the paper in the context of the observed defect reactions.

D-VIII.05 12:20

DIFFUSION SPECTROSCOPY WITH ISOTOPICALLY CONTROLLED SEMICONDUCTORS

H. Bracht Institute of Materials Physics, University of Muenster, 48149 Muenster, Germany, H.H. Silvestri, I.D. Sharp, E.E. Haller, Department of Materials Science and Engineering, University of California Berkeley, and Lawrence Berkeley National Laboratory, Berkeley CA, 94720, USA

A general method to investigate the nature and properties of native point defects in materials at high temperatures is "diffusion spectroscopy". On first sight this appears to be an oxymoron but diffusion studies can in fact be performed in such a way that detailed information about native point defects and their impact on foreign-atom diffusion is accessible.

Isotopically controlled silicon heterostructures serve as ideal test structures to follow the depth-dependent self-diffusion, which can result from the diffusion of foreign-atoms into the isotope structure and their reactions with the host atoms and vacancies. In particular, the incorporation of dopants to concentrations that exceed the intrinsic carrier concentrations makes the material extrinsic. As a consequence, the position of the Fermi level is affected and therewith the thermal equilibrium concentration of charged native point defects. In this contribution we highlight our results on boron, phosphorous, and arsenic diffusion in silicon isotope multilayer structures. It is demonstrated that the simultaneous diffusion of self- and dopant atoms provides new information about the mechanisms of self- and dopant diffusion and the properties of the native point defects involved which are not accessible by self- and dopant diffusion experiments performed separately.

12:35 **LUNCH**

Session IX : Dopant diffusion/activation
Session chair: W. Lerch

D-IX.01 14:05 -Invited-

BORON DIFFUSION IN STRAINED AND STRAIN-RELAXED SiGe

C.C. Wang, T.Y. Huang, Y.M. Sheu, Sally Liu, Device Engineering Division, TSMC, Carlos H. Diaz, Logic Technology Division, TSMC, Ray Duffy, Anco Heringa, Philips Research Leuven, Belgium, N.E.B. Cowern, University of Surrey, Guildford, U.K., Peter B. Griffin, CIS, Stanford University, USA

Strain engineering has become a popular approach to improve device performance recently. Strained SiGe deposition is one of the approaches to create strain in critical region of device. Boron diffusivity under this circumstance has been modelled with a diffusivity retardation that is an exponential function of the strain. Alternatively, it is also claimed that the retardation is from Ge-B pairing instead. A quantitative assessment of the respective contribution from mechanical strain and Ge doping is therefore necessary for accurate boron modeling in SiGe.
We performed two experiments with strained and strain-relaxed SiGe respectively. Ultra-shallow boron junctions were created with low energy implant and following RTA anneal in both two experiments. Both boron and germanium profiles were analyzed by secondary ion mass spectrometry (SIMS) after the process was completed. The first step in modelling procedure is to fit the retarded B diffusion in strain-relaxed SiGe with a Ge concentration and anneal temperature dependent empirical equation. It is derived from a temperature dependent Ge-B pairing model. Secondly, to fit the retarded B diffusion in strained SiGe by both the empirical equation and a strain dependent activation energy of diffusivity. The strain dependent increase in the activation energy was extracted. A detailed diffusivity retardation component under both mechanical strain and Ge doping is therefore investigated with these two models. The retardation effect from mechanical strain still plays a significant role in strained SiGe. Summarily, this paper describes the experiments, calibration and resulting diffusion constants for an ultra-shallow boron junction that is popular in advanced CMOS technology.

D-IX.02 14:35

THE EFFECT OF BIAXIAL STRAIN ON IMPURITY DIFFUSION IN Si AND SiGe

A. Nylandsted Larsen(a), N. Zangenberg(a,b), and J. Fage-Pedersen(a,c), (a)Institute of Physics and Astronomy, University of Aarhus, 8000 Aarhus C, Denmark, (b)Molecular Beam Epitaxy Laboratory, University of British Columbia, (c)Research Center COM, Techn Univ of Denmark

The introduction of strain in active device areas offers significant improvements of the performance of CMOS circuits, and research is ongoing worldwide to improve the fabrication schemes of the strained layers and to characterize them physically. It is of crucial importance for the simulations of strained CMOS devices that reliable experimental information exists against which the simulation models can be tested.
We will present results from diffusion studies of different impurities in biaxially strained Si and Si(1-x)Ge(x)for low x-values. The structures are MBE grown on strain-relaxed Si(1-x)Ge(x) layers, and the impurity profiles were introduced during growth. We have in particular been concerned with the effect of biaxial strain on the diffusion of pure vacancy-assisted diffusers (Sb and, partly, Ge) and pure interstitial-assisted diffusers (B and P). We have found that compressive biaxial strain retards the diffusion of the interstitial-assisted diffusers, whereas tensile biaxial strain enhances the diffusion of these impurities. The opposite is the case for the vacancy-assisted diffusers. The activation energy for vacancy-assisted diffusion is not strongly influenced by the strain, which is opposite to the situation for interstitially assisted diffusion.

D-IX.03 14:50

STRAIN EFFECTS ON TRANSIENT ENHANCED DIFFUSION IN AS-IMPLANTED ULTRASHALLOW JUNCTIONS

G.D.M. Dilliway(a), A.J. Smith(a), J.J. Hamilton(a), L. Xu(b), P.J. McNally(b), G. Cooke(c), H. Kheyrandish(c), N.E.B. Cowern(a), (a)Advanced Technology Institute, University of Surrey, Guildford Surrey GU2 7XH, U.K., (b)School of Electronic Engineering, Dublin City University, Dublin 9, Ireland, (c)MATS-UK, Innovation House, Birchwood, Warrington WA3 6UT, U.K.

To control and optimise strain engineering in advanced CMOS it is important to understand strain effects on doping. In this work the effects of strain on transient enhanced diffusion (TED) in As-implanted ultrashallow junctions are presented.

Experiments on the thermal equilibrium diffusion of dopants in strained Si layers have shown significant strain effects, but up to now no study has investigated the impact of strain on the transient enhanced diffusion arising during annealing of implantation damage in strained Si layers. In this study, implantation and annealing experiments were performed using tensile biaxially-strained Si layers grown on SiGe strain-relaxed buffer layers by low-pressure chemical vapour deposition. Unstrained Si control wafers were also prepared using the same growth process. After epitaxy, wafer pieces were implanted with 3 keV, 4 x 1014/cm2 As and annealed in dry N2 at temperatures in the range 650-950°C for 10s up to 104s. Samples were characterized by SIMS to measure atomic concentration profiles, by four-point probe and Hall measurements to determine sheet resistance and mobility, and by TEM to determine microstructure. Tensile strain was found to increase both the magnitude and timescale of TED, consistent with stabilisation of two types of interstitial defects - first, the end-of-range extended defects which act as the source of interstitials driving TED, and second, the As interstitial pairs which are the dominant diffusing As species during TED. This stabilisation of interstitial defects is a natural consequence of the volume change associated with strain. Concentration-enhanced As diffusion, driven by vacancies, is correspondingly suppressed in the tensile-strained material.

D-IX.04 15:05

BORON DIFFUSION IN AMORPHOUS SILICON

V.C. Venezia, Axcelis Technologies, Beverly MA 01915, USA, R. Duffy, Philips Research, 3001 Leuven, Belgium, L. Pelaz, University of Valladolid, 47011 Valladolid, Spain, M.J.P. Hopstaken, G.C.J. Maas, T. Dao, Y. Tamminga, and P. Graat, Philips Research, 5656 AA Eindhoven, The Netherlands

Solid-phase-epitaxy-regrowth (SPER) has gain considerable interest as a junction formation method in advanced CMOS technologies because it produces highly-active, shallow junctions at low temperature (<700C). Recent work has shown that B profiles broaden during SPER. Although some aspects of this B diffusion in amorphous silicon (a-Si) are known, the high rate of SPER provides only a small temperature-time frame to study this effect. Unlike previous investigates, this work employed silicon-on-insulator (SOI) substrates in which the entire silicon over layer was amorphized with a Ge implant prior to B implantation. The lack of an amorphous/crystal interface prevented SPER, extending the temperature-time range of this study. Dopant profiles were analyzed by SIMS, while TEM and X-ray diffraction were used for structural characterization; allowing for the exclusion of samples in which the onset of poly-crystalline formation occurred. As in crystalline silicon, B diffusion in a-Si exhibited a square-root time dependence and an exponential dependence on temperature. An activation energy of approximately 2.8eV was calculated. This value is significantly lower than that obtained for equilibrium B diffusion in crystalline silicon (3.5eV) and only slightly larger than SPER (Ea~2.4-2.7eV). With these results a more predictive model for B junction formation by SPER is possible.

D-IX.05 15:20

BORON DIFFUSION IN PRESENCE OF DEFECTS INDUCED BY HELIUM IMPLANTATION

F. Cayrel(a), D. Alquier(a), C. Dubois(b) and R. Jérisian(a), (a)Université de Tours, L.M.P., 16 rue Pierre et Marie Curie, BP 7155, 37071 Tours cedex 2, France, (b)L.P.M. - INSA Lyon, 20 rue A. Einstein, 69621 Villeurbanne Cedex, France

Among numerous metallic impurities gettering techniques, helium implantation that leads to the formation of both defect types (interstitial and vacancy type) has been investigated. The gettering efficiency has been demonstrated for metals like Au, Ni, Cu or Fe. Moreover, gettering of dopant has also been observed on these defects. Boron is of particular interest for the realisation ultra-shallow junctions and its interactions with interstitial type defects are widely studied. In this paper, we will particularly focus our attention on boron diffusion in presence of He induced defects. The Boron diffusion, known to be driven by interstitial mechanism, can be largely affected by the presence of cavities, which are sinks for interstitial, as well as dislocations or rod-like defects that can be considered as interstitial sources. In this work, N-type <111> Si wafers doped at 1x1014 B.cm-3 were implanted with helium for various doses [1-5]x1016 He+/cm2 and energies [40-160]keV. Boron implantation was then performed at 5keV for a dose of 2x1013 B.cm-2. Secondary Ion Mass Spectroscopy (SIMS), Transmission Electron Microscopy (TEM) and simulation with PROMIS 1.5 code were used in order to study the defect band impact on boron diffusivity after classical thermal treatment. as a The impact of various parameters on boron diffusivity, such as defect density, distance between boron profile and defect band or annealing temperature is discussed in this work.

D-IX.06 15:35

BORON DISTRIBUTION IN SILICON AFTER EXCIMER LASER ANNEALING WITH MULTIPLE PULSES

E.V. Monakhov and B.G. Svensson, Department of Physics/SMN, University of Oslo, PO Box 1048 Blindern, 0316 Oslo, Norway, M.K. Linnarsson, Solid State Electronics, Royal Institute of Technology, Stockholm, Sweden, A. La Magna, M. Italia and V. Privitera, CNR-IMM, Catania, Italy, G. Fortunato, M. Cuscunà and L. Mariucci, CNR-IFN, Rome, Italy

We have studied B re-distribution in Si after excimer laser annealing (ELA) with multiple laser pulses. B was implanted with energies of 1 and 10 keV and doses of 1x1014 and 1x1015 cm-2. ELA with the number of pulses from 1 to 100 was performed in vacuum with the sample kept at room temperature and 450oC. Chemical B concentration and electrical activation profiles were measured by secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP), respectively. Structural studies of the samples have been done using transmission electron microscopy (TEM), including high-resolution TEM (HRTEM). Independently of the implantation parameters and the ELA conditions used, a peak in the B concentration is observed by SIMS near the maximum melting depth after 10 pulses of ELA. A detailed study has revealed that B accumulates at the maximum melt depth gradually with the number of ELA pulses. An increase in the carrier concentration at the maximum melt depth is observed by SRP after ELA with 100 pulses. No structural defects have been detected by TEM and HRTEM in the region of the B accumulation. Formation of Si-B complexes or nuclei, with sub-critical size, of a new phase during ELA is suggested.

15:50 **BREAK**

Session X : Defect/strain characterisation
Session chair: M. Foad

D-X.01 16:10

CHARACTERISATION OF 311 DEFECTS IN PRE-AMORPHISED SILICON BY GRAZING INCIDENCE DIFFUSE X-RAY SCATTERING

L. Capello(a), T.H. Metzger(a), K. Nordlund(b), F. Cristiano(c), W. Lerch(d), P. Calvo(e), S. Paul(d), (a)E.S.R.F., BP 220, 38043 Grenoble, France, (b)University of Helsinki, P.O. Box 43, 00014 Helsinki, Finland, (c)LAAS/CNRS, 7, Avenue du Colonel Roche, 31077 Toulouse, France, (d)Mattson Thermal Products GmbH, Daimlerstr. 10, 89160 Dornstadt, Germany, (e)CEMES/CNRS, 29 Rue Jeanne Marvig, 31055 Toulouse, France

Ion implantation is an important processing tool in Si based CMOS technology. Amorphising Si by ion implantation originates a Si interstitial (SiI’s) supersaturation with associated end-of-range (EOR) damage below the amorphous to crystalline interface. During subsequent annealing at high temperature, needed to recover the crystalline structure and activate the dopant, the SiI's form different kind of extrinsic defects like “magic clusters”, 311 defects, faulted and perfect dislocation loops (DL’s) [1]. Recently, synchrotron-based techniques were developed to investigate this kind of defects, e.g. grazing incidence-diffuse x-ray scattering (GI-DXS) was successfully applied to study DL’s [2]. Based on atomistic simulations for DXS [3], we report here on the characterisation of 311 defects. We studied their evolution in Ge pre-amorphised Si samples during isothermal annealing at 800°C [4]. We observed that the predominant 311 defect is of 1HexZD type [3]. The defects grow in time both in width and length and partially transform into faulted DL’s for longer annealing time. An exponential decay of the number of Si interstitials bound into 311 defects was found along with the growth of DL’s and the annihilation of SiI’s at the surface.

This research was supported by EU grant IMPULSE: IST-2001-320061

1 A. Claverie, B. Colombeau, B. De Maudit, C. Bonafos, X. Hebras, G. Ben Assayag, F. Cristiano, Appl. Phys. A, 76, 1025 (2003). 2 L. Capello, T. H. Metzger, Mat. Sci. Eng. B, 114-115, 77 (2004).
3 K. Nordlund, J. Appl. Phys., 91, 2978 (2002).
4 W.Lerch, S. Paul, J. Niess, F. Cristiano, Y. Lamrani, P. Calvo, N. Cherkashin, D. F. Downey, E. A. Arevalo, Electrochem. Soc. Proceedings, 2004-01, 90 (2004).

D-X.02 16:25

DISLOCATION-IMPURITY INTERACTION IN Si

I. Yonenaga, Institute for Materials Research, Tohoku University, Sendai 980-8577, Japan

Understanding dislocation-impurity interaction is important for advanced silicon technology. There are two aspects: (1) dislocation effect on the spatial distribution of impurities, such as gettering, defect reaction and complex formation, which is essential for dislocation-engineering; (2) impurity effect on the dynamic activity of dislocations, which is key to grow dislocation-free crystals and suppress slip and warpage during wafer processing. However, except for oxygen impurity, far less is known on dislocation-impurity interaction in Si doped with other impurities. This paper reports on the dynamic interaction in Si doped with light impurity (N), acceptor (B, Ga), donor (P, As, Sb) and neutral (Ge) impurities to various concentrations up to 2.5*1020 cm-3.

B, P and As impurities suppress the dislocation generation at elevated temperatures remarkably when the concentrations exceed 1*1019 cm-3, while Ge impurity has not a strong suppression effect of dislocation generation. Dislocations are immobilized by the impurity segregation and stable complex formation by defect reaction. Dislocation velocity in Si doped with P, As and Sb impurities increases with increase in the concentration. Similarly, B impurity leads to the enhancement and neutral impurity Ge increases slightly. The velocity enhancement is attributed to the electrical effect of donor or acceptor impurities through the formation and/or migration of kinks as an elementary process of dislocation motion.

D-X.03 16:40

QUANTITATIVE STRAIN AND STRESS MEASUREMENTS IN ALTERNATING Ge/Si THIN LAYERS GROWN BY CVD ON A RELAXED Si0.5Ge0.5 BUFFER LAYER

N. Cherkashin, M.J. Hÿtch, E. Snoeck, A. Claverie, CEMES-CNRS, 29 rue J. Marvig, 31055 Toulouse, France, J.M. Hartmann, CEA-DRT, LETI/D2NT & DPTS, CEA – GRE, 17 avenue des Martyrs, 38054 Grenoble Cedex, France, Y. Bogumilowicz, STMicroelectronics, 850 rue Jean Monnet, 38921 Crolles Cedex, France

The incorporation of new compound materials of IV-IV type (Si, Ge) into MOS channels is a promising route for creating ultimate Si-based devices. The 4.2% lattice mismatch between Si and Ge means that Si1-xGex layers grown on a Si substrate are strained. By alternating thin layers of Ge under compression/Si under tension, it is possible to considerably increase the mobility of spatially confined holes/electrons. Consequently, understanding and manipulating the strain is now a natural prerequisite for device applications of Si1-xGex/Si heterostructures. In this work we performed quantitative measurements of strain in a structure consisting of two 7 nm-thick strained Ge and Si layers subsequently grown by CVD on a relaxed Si0.5Ge0.5 buffer layer. Particular attention was paid to the characterization of defects within all these layers by making use of Weak Beam TEM imaging. Geometric Phase Analysis of High Resolution (HR) TEM images was used to measure the strain within Ge and Si layers. In practice, it consists in measuring the atomic plane displacement from reference buffer layer Si0.5Ge0.5 lattice after Fourier processing of a HR TEM image. The in-plane stress within each layer was deduced. Experimental results were compared with the predictions of elasticity theory and discussed in terms of effect of defect formation.

D-X.04 16:55

XRD ANALYSIS OF STRAINED Ge-SiGe HETEROSTRUCTURES ON RELAXED SiGe GRADED BUFFERS GROWN BY HYBRID EPITAXY ON Si(001) OFF-CUT SUBSTRATES

N. Franco, N.P. Barradas, E. Alves, Instituto Tecnológico e Nuclear, E.N. 10, 2685-953 Sacavém, Portugal, R.J.H. Morris, T.J. Grasby, O.A. Mironov, E.H.C. Parker, Department of Physics, University of Warwick, Coventry CV4 7AL, U.K.

Ge/Si1-XGeX inverted modulation doped heterostructures with Ge channel thickness of 16 nm and 20 nm were grown by a method of hybrid epitaxy followed by ex-situ annealing at 650 C for p-HMOS application. The thicker layers of the virtual substrate (6000 nm graded SiGe up to X=0.6 and 1000 nm uniform composition with X=0.6) were produced by ultrahigh vacuum chemical vapor deposition (UHV-CVD) while the thinner, Si(2nm)-SiGe(20 nm)-Ge-SiGe(15 nm+ 5 nm B-doped +20 nm) active layers were grown by low temperature solid source (LT-SS) MBE at T=350C. As grown and annealed samples were measured by X-ray diffraction (XRD). Reciprocal space maps allowed us to determine nondestructively and precisely the composition and strain of the channel, as other layers for the whole structure. Layer thickness and roughness was determined with complementary high-resolution Rutherford backscattering (RBS) experiments. We relate XRD and RBS parameters with XTEM and plan-view TEM results to confirm off-cut orientation and upper interface channel roughness values.

17:10-19:00 **POSTER SESSION II**

POSTER SESSION II

Thursday, June 2, 2005
17:10 – 19:00

Session chair: F. Giannazzo

D/PII.01 INJECTION OF POINT DEFECTS DURING ANNEALING OF LOW ENERGY AS IMPLANTED SILICON

C. Tsamis(a), D. Skarlatos(a), V. Valamontes(b), D. Tsoukalas(C), G. BenAssayag(c), A. Claverie(c) and W. Lerch(e), (a)IMEL/NCSR "Demokritos", 15310 Aghia Paraskevi, Athens Greece, (b)Department of Electronics, Technological and Educational Institute of Athens 122-10 Aegaleo, Greece, (c)Faculty of Applied Mathematical and Physical Sciences, NTUA, 157 80 Athens, Greece, (d)Toulouse Ion Implantation Group, CEMES/CNRS, 29 rue J.Marvig, 31055 Toulouse, France, (e)Mattson Thermal Products GmbH, Daimlerstr. 10, D-89160 Dornstadt, Germany

High-dose, low energy arsenic implantation is a process that is typically used for the formation of S/D regions in silicon transistors. Compared to other dopants such boron and phosphorus, fewer studies have been performed for the Transient Enhanced Diffusion (TED) of arsenic. Three sources have been identified for point defects injection that can contribute to the TED of arsenic and result in interstitial injection into the substrate. These sources are: a) the end-of-range damage, b) arsenic clustering and c) arsenic precipitation. Moreover, as the implantation energy is reducing and the implanted profiles are moving closer to the surface, the influence of the surface would be more severe.

In this work we investigate the damage generated by low-energy high dose As implantation performed at room temperature. The approach consists in monitoring the diffusion of the Arsenic profile as well as of Boron profile in buried δ-doped layers. Silicon wafers containing two boron delta - layers at depth of 0.6 and 1.1 um respectively were implanted with arsenic at various energies and dose. The wafers were annealed by RTA at 900oC for 5 and 30 sec in N2 ambient. RTA anneals were performed by Mattson. SIMS analysis was performed for both Boron and Arsenic profiles, using the appropriate conditions in each case. The experimental results indicate that the contribution of the implantation damage to the TED of As and B is not the main one. On the contrary, interstitial injection due to As clustering is more important for the present conditions. From the analysis of the diffusion profiles we have estimated the value of the supersaturation ratio of silicon interstitials, consistent for both dopants.

D/PII.02 INTERSTITIAL INJECTION DURING OXIDATION OF VERY LOW ENERGY NITROGEN - IMPLANTED SILICON

D. Skarlatos and C. Tsamis, IMEL, NCSR “Demokritos”, 15310 Aghia Paraskevi, Athens, Greece, M.Perego and M.Fanciulli, INFM – Laboratorio MDM, Via Olivetti 2, 20041 Agrate Brianza (Milano), Italy

Oxidation of nitrogen - implanted silicon is one of the methods developed in order to incorporate nitrogen within the growing thermal oxide in order to improve its reliability in the ultra thin (< 4 nm) regime. The main advantage of the method is that enables the formation of various oxide thickness across the silicon substrate - by performing local nitrogen implantations of various dose and using one single oxidation step. This is very helpful for Systems On Chip fabrication [1].

It is also known that oxidation of silicon causes an interstitial injection into the silicon substrate, which enhances the diffusivity of dopants, as boron and phosphorus, which diffuse via an interstitial - mediated mechanism [2]. In this article we present a study of interstitial injection during oxidation of very low energy nitrogen implanted silicon using boron δ - layers as interstitial monitors. No interstitial injection enhancement in comparison to common dry oxidation was observed. This result is different from N2O oxynitridation [3], during which an enhancement of interstitial injection of the order of 25% was observed, revealing the influence of interfacial nitrogen on interstitial kinetics. The most probable explanation, supported by a variety of other experiments, is that implanted nitrogen acts as an interstitial sink. In particular it seems that nitrogen "captures" the excess interstitials produced by implantation and oxidation for his non - Fickian diffusion towards the surface. [1] J-P.Carrere, A.Grouillet, F.Guylader, A.Beverina, M.Bidaud, A.Halimaoui, ESSDERC 2002, 155. [2] P.M. Fahey, P.B.Griffin and J.D.Plummer, Rev. Mod. Phys., 61(2), 289, (1989) [3] D.Skarlatos, D.Tsoukalas, L.F.Giles and A.Claverie, J. Appl. Phys., 87(3),1103, (2000).

D/PII.03 ARSENIC DIFFUSION IN GERMANIUM

S. Brotzmann and H. Bracht, Institute of Materials Physics, University of Muenster, 48149 Muenster, Germany

We have performed arsenic diffusion experiments in germanium at temperatures between 640°C and 920°C utilizing an As-Ge alloy source with less than 1at% arsenic. The low arsenic content in the source avoids a strong degradation of the specular surface of the germanium sample during close ampoule annealing which was otherwise observed for As-Ge sources with higher arsenic contents. After annealing diffusion profiles of arsenic were recorded by means of spreading resistance profiling (SRP). In order to calculate arsenic concentrations the spreading resistance profiles were first converted to resistivity profiles with the help of homogeneously doped samples with well-known resistivities. Then arsenic concentrations were calculated taking into account the donor level of arsenic in germanium. For our calculation we assume that the spreading resistance measured after diffusion is mainly caused by arsenic dissolved on substitutional lattice sites. The concentration profiles of arsenic exhibit a box shape which is similar to the shape of arsenic profiles in silicon. Numerical simulations on the basis of appropriate diffusion mechanisms show that arsenic diffusion in germanium is most likely mediated by a vacancy mechanism. Our results obtained for the diffusion and properties of the point defects involved are discussed against the background of the present understanding on atomic mass transport processes in germanium.

D/PII.04 PHOSPHORUS DIFFUSION INTO SILICON AFTER VAPOR PHASE SURFACE ADSORPTION OF PHOSPHINE

Bodo Kalkofen, Marco Lisker, Edmund P. Burte, Institute of Micro and Sensor Systems, Otto-von-Guericke-University of Magdeburg, 39016 Magdeburg, Germany

Shallow phosphorus doping of silicon was carried out by using a damage-free two-step doping process. Phosphorus was deposited on to the silicon surface by self-limited dissociative adsorption of phosphine from the gas phase. Diffusion and activation of the phosphorus was performed by succeeding conventional rapid thermal lamp annealing in a low pressure oxygen atmosphere. Different deposition and annealing conditions, as well as the influence of the oxide coverage were investigated.

The sheet resistance, the oxide thickness, and the phosphorus concentration were analysed by four point probe measurements, ellipsometry, and secondary ion mass spectroscopy (SIMS), respectively. Annealing at different temperatures above 850 °C for 10 s resulted in junction depths of 55 nm to 122 nm with sheet resistances of 1150 to 620 Ohm/sq, respectively. The SIMS measurements revealed a Gaussian doping profile and a peak of the phosphorus concentration close to the surface of the as-doped samples while the piled-up phosphorus almost disappeared with the oxide removal in an HF-dip. The trapped phosphorus appeared to be inactive as inferred from comparison of the sheet resistance measurements and calculations of the sheet resistance from the profiles. The phosphorus movement and activation are assumed to be due to detrapping - as it is also observed in the reverse dose loss effect of annealed implanted samples - and oxidation enhanced diffusion.

D/PII.05 **D-IX.05**

D/PII.06 BORON INTERACTION WITH EXTENDED DEFECTS INDUCED BY He-H Co-IMPLANTATION IN Si

G. Gaudin(a), F. Cayrel(a), C. Bongiorno(b), R. Jérisian(a), C. Dubois(c), V. Raineri(b) and D. Alquier(a), (a)Université de Tours, L.M.P., 16 rue Pierre et Marie Curie, BP 7155, 37071 Tours cedex 2, France, (b)CNR-IMM, Stradale primosole, 50, 95121 Catania, Italy, (c)L.P.M. - INSA Lyon, 20 rue A. Einstein, 69621 Villeurbanne Cedex, France

Helium and hydrogen implantations lead to the formation of extended defects that strongly interact with impurities like metal and dopants, affecting significantly their final profile. Even if the efficiency of this gettering technique is widely demonstrated in literature, the high doses required are uncompatible with industrial applications. Dose reduction becomes then crucial. In the smartcut(r) process, it has been shown that helium and hydrogen co-implantation leads to the expected dose decrease. The same idea was then applied for the gettering technique, keeping co-implantation doses below exfoliation threshold.

After evidencing the impact of the H addition on gettering efficiency, this paper will focussed on boron interactions with He-H induced defects. For this purpose, uniformly high doped (1018B.cm-3) P-type <111> wafers were used. He implantation at 40keV for a dose of 11016 He+.cm-2 followed or not by H implantation at 35keV for different doses were carried out. Samples were subsequently furnace annealed for 1h at temperatures ranging from 500°C to 900°C. Secondary Ion Mass Spectrometry (SIMS) was used to follow the boron and hydrogen profiles while the Transmission Electron Microscopy (TEM) observations allow us to monitor the defects evolution. This work enlighten the large impact of H on cavity growth. Moreover, our results clarify the interaction of B with extended defects induced by a He-H co-implantation.

D/PII.07 SUBSTRATE INFLUENCE ON THE OUTDIFFUSION OF ANTIMONY DOPANT IN MONOCRYSTALLINE SILICON

R. Labbani and R. Halimi, Laboratory of Thin Films and Interfaces, Department of Physics, Faculty of Sciences, University Mentouri of Constantine, Route de Ain el Bey, 25000 Constantine, Algeria

In this work, we study the effect of silicon substrate orientation on the outdiffusion of antimony dopant. The monocrystalline Si(100) and Si(111) substrates were implanted with Sb+ ions at an energy of 60 keV, to a dose of 5×1015 Sb+cm-2. The recovery of radiation damage was performed with a conventional annealing treatment at 900°C. The analysis was carried out by means of high resolution RBS (Rutherford backscattering spectroscopy) technique using protons of 0.3 MeV energy.

It was shown that Sb+ ions were rejected to the surface, for both Si(100) and Si(111) samples. Moreover, it was noticed that an important quantity of antimony was lost especially for the case of Si(111) specimens. Finally, we note that several ion implantation parameters (Rp, DRp, dose, radiation damage) were evaluated with a good accuracy.

D/PII.08 POROUS SILICON DAMAGE ENHANCED PHOSPHOROUS AND ALUMINIUM GETTERING OF p TYPE CZOCHRALSKI SILICON

M. Hassen, A. Ben Jaballah*, M. Hajji, H. Rahmouni, B. Bessais, A. Selmi, H. Ezzaouia, Institut National de Recherche Scientifique et Technique, Laboratoire de Photovoltaïque et des Semiconducteurs, PB 95 2050 Hammam-Lif, Tunisia, b Laboratoire de Physique des Semiconducteurs et des Composants Electroniques Faculté des Sciences de Monastir, Rue de Kairouan 5000 Monastir, Tunisia

Ion implantation and mechanical damage are widely used as a preliminary step to getter unwanted impurities and extended defects in Czochralski type silicon. In this work, porous silicon damage (PSD) is introduced like a simple setup for efficient external purification sequences. The method consists to create thin nanoporous p-type silicon on both sides of the silicon substrates with randomly hemispherical voids. Then, two main sample types are processed: for the first set, thin aluminium layers (≥1 µm) are thermally evaporated followed by photo-thermal annealing treatments, for the second set, phosphorous is continually deposited in a solid phase from POCl3 solution during heating at one of several temperatures ranging between 750 °C and 1000 °C for 1 h, in nitrogen ambient for silicon substrates with and without porous silicon damage. Metal / oxide (SiO2) / Si structures are elaborated to extract the minority diffusion length (Ln) from Light Beam Induced Current measurements (LBIC). In both cases, the results show the existence of an optimum gettering temperature. PSD enhanced Phosphorous diffusion gettering and allow obtaining Ln of about 190 µm. In this study, we either demonstrates that enhanced metal solubility model can not explain the gettering effect. The solid solubility of aluminium is higher than that of P atoms; however, the device yield confirms the effectiveness of P as compared to Aluminium. Photo-current investigations for shallow N+PP+ junctions confirm these results.

D/PII.09 PLATINUM IN-DIFFUSION CONTROLLED BY RADIATION DEFECTS FOR ADVANCED LIFETIME CONTROL IN HIGH POWER SILICON DEVICES

P. Hazdra and J. Vobecký, Department of Microelectronics, Czech Technical University in Prague, Technická 2, 16627 Prague 6, Czech Republic

The low-temperature (~700°C) in-diffusion of platinum (Pt) into the n-type float zone silicon guided and enhanced by radiation damage produced by implantation of helium ions was used to shape the profile of ideal recombination centers - platinum substitutionals (Pts). Single and multiple energy implantation of helium ions with energies up to 15 MeV introducing different profiles of radiation defects were applied for this purpose. Both the platinum silicide (PtSi) and implanted Pt layers were compared as the sources of Pt diffusion. The full-depth distribution of in-diffused Pt was studied by monitoring the acceptor level of Pts-/0 (EC-ET=0.23eV) by the current transient spectroscopy. Results show that the helium implantation significantly enhances platinum diffusion and allows its control up to the depths of hundreds of micrometers. The resulting Pts distribution can be controlled by the profile of radiation damage produced by helium ions while the amount of in-diffused Pts is set by the dose of platinum implantation. Application of the method using both the implanted and PtSi sources will be shown on optimization

of turn-off properties of high power P-i-N diodes. Advantages and drawbacks of the both approaches will be discussed, as well.

D/PII.10 ULTRA SHALLOW N+P JUNCTIONS FORMED BY Sb IMPLANTATION INTO BULK SILICON AND SOI SUBSTRATES

D. Girginoudi, Department of Electrical and Computer Engineering, Democritus University of Thrace, 67100 Xanthi, Greece

Ultra shallow n+p junctions with low sheet resistance are required to realize sub100-nm NMOSFETS. Sb ion implantation is suitable for the fabrication of even shallower junctions, with more lateral junction abruptness, compared to As. Sb does not exhibit the transient enchased diffusion (TED) induced by implant damage, observed with P and As, which diffuse through a Si self-intertitial mechanism, because Sb is a vacancy diffuser in silicon. However, it has been shown that its electrical activation decreases significantly with increasing thermal budget, due to precipitation and out-diffusion of Sb. On the other hand, the formation of ultra shallow n+p junctions for the fabrication of NMOSFETS on silicon -on -insulator (SOI) subtrates by Sb ion implantation has not as yet sufficiently studied.
In this work we investigate the Sb dopant behavior and damage in (100) oriented p-type bulk and SOI substrates. Sb was implantated at 5keV/1e15cm-2 into both these substrates. Some of the substrates were preamorphised by Ge implantation. The implanted samples were subjected to thermal annealing at 600oC and 950oC for different annealing times. ToF-secondary ion mass spectrometry and sheet resistance measurements were carried out to study both the dopant diffusion and electrical activation. A study of depth distribution of residual defects was done using Transmission Electron Microscopy (TEM). The results of this investigation, regarding the damage, dopant diffusion, and dopant activation/deactivation in both bulk and SOI substrates, will be presented and discussed.

D/PII.11 STRUCTURAL AND ELECTRICAL CHARACTERIZATION OF DEFECTS INTO P+N JUNCTIONS FORMED BY Ge-PREAMORPHISED SILICON WITH LOW AND HIGH THERMAL BUDGET

D. Girginoudi, S. Matziris, N. Georgoulas and A. Thanailakis, Department of Electrical and Computer Engineering, Democritus University of Thrace, 67100 Xanthi, Greece

Low energy B or BF2 ion implantation into amorphous Si, preamorphised by Ge ion implantation, allows ultra shallow p+n junction formation. Recently, F co-implantation has been used as an alterative method, and the effect of F on the junction depth has been studied. However, the above process is known to generate defects such as dislocations, vacancies and interstitials which can induce electrically active deep levels into the Si bulk, which may increase the generation current in the depletion region acting as generation-recombination sites for carriers. The formation and the electrical properties of these defects have not previously been sufficiently studied. In this work p+n junctions have been obtained using three approaches by ion implantation into Ge preamorphised Si: (i) 1keV/1e15cm-2 B implantation, (ii) 4.5keV/1e15cm-2 BF2 implantation, and (iii) 10keV/1e15cm-2 F co-implantation followed by 1keV/1e15cm-2 B implantation. Low temperature annealing at 600oC, as well as high temperature annealing at 950oC was performed. The characterization of deep levels has been carried out using deep level transient spectroscopy (DLTS) and isothermal transient capacitance ΔC (t, T) measurements. Furthermore, in order to determine the nature of defects in the end of range (EOR) region, transmission electron microscopy (TEM) measurements were carried out. Analysis of DLTS spectra has shown the existence of deep levels associated with secondary defects. The EOR defects influence the electrical activity of these defects. The results of this investigation, regarding the stability factor of deep levels introduced by different ion implantation technological steps, and the effect of annealing conditions on the defect structure and their density, will be presented and discussed.

D/PII.12 POSITRON ANNIHILATION STUDIES OF HIGH DOSE Sb IMPLANTED SILICON

H. Schut, S.W.H. Eijt, Department of Radiation, Radio-nuclides & Reactors, Faculty of Applied Sciences, Delft University of Technology, Mekelweg 15, 2629 JB Delft, The Netherlands, C.D. Beling, K. Ho, Department of Physics, University of Hong Kong, Pokfulam Road, Hong Kong, P.R. China and Y. Takamura, University of Califoria, Berkeley CA 94720, USA

The formation and evolution of vacancies and precipitates created by implantation of 60 keV, 2x10^16 cm^-2 Sb^+ in pre-amorphized (001) Cz-Si is studied using the Doppler Broadening (DB) and two-dimensional Angular Correlation of Annihilation Radiation (2D-ACAR) positron beam techniques. After implantation, samples were laser annealed (LTA) and subsequently thermal annealed at temperatures ranging from 400 to 1000 C. Implantation-induced vacancy type defects were detected up to a depth of 280 nm. After LTA, positron annihilation related to both Sb and remaining defects is observed in the first 100 nm below the surface. The deeper region only shows positron trapping at vacancy-type defects with strong reduced concentration. Complete removal is obtained after 600 C anneal. At this temperature, the positron data for the upper region reveals trapping at Sb and Si sites only. With increasing annealing time (at 600 C) or increasing temperature (up to 1000 C) positron annihilation at Sb-sites associated with neighboring vacancies becomes apparent. Results will be correlated with the observed Sb electrical deactivation above 600 C, the shift from small Sb aggregates to precipitates and out-diffusion of Sb from the implantation region at higher temperatures.

D/PII.13 ROOM-TEMPERATURE BORON DISPLACEMENT IN CRYSTALLINE SILICON INDUCED BY PROTON IRRADIATION

Alberto Maria Piro, Lucia Romano, Salvatore Mirabella, Maria Grazia Grimaldi, MATIS-INFM and Dipartimento di Fisica e Astronomia, Università di Catania, 64 via S. Sofia, 95123 Catania, Italy

B off-lattice displacement under energetic proton beam (300¸2000keV) irradiation was studied on crystalline Si, grown by MBE and uniformly doped with 1E20 B/cm3. B, fully substitutional in the as-grown sample, was detected by channelling analyses along the <100>, <110> crystalline axes, using the 11B(p,a)8Be nuclear reaction at the energy of 650 keV. The normalized B yield, c, is shown to increase with the ion fluence saturating at a value cF<1, depending on the channeling axis. Thus, B is kicked out at room temperature from its lattice position but it is not randomly located in the Si lattice. Detailed simulations indicate the formation of a B-B pair upon a single lattice site, with B atoms displaced along the <100> direction, the one by 1.25 Å and the other by -0.30 Å with respect to the substitutional site. We showed that the B displacement is caused by the Si self-interstitials (ISi) locally generated in the lattice by the irradiating beam, which, in addition, favours the B diffusion by means of the B-ISi couples (highly mobile also at room temperature). Since Si interstitials produced in the B doped layer contribute to the B displacement, we fit the damage rate by the following formula c=cF-[cF-c0]*exp(-s*NI), where c0 is the c of the as-grown sample and NI is the ISi fluence calculated by TRIM. By this exercise, we extracted the room temperature ISi-B interaction cross section to be s~10-16 cm2.

D/PII.14 ATOMIC AND ELECTRONIC STRUCTURE OF VACANCY-PHOSPHORUS COMPLEXES IN STRAINED SiGe LAYERS

K. Saarinen(a,b), S.W.H. Eijt(a), J. Slotte(b) and H. Schut(a), (a)Department of Radiation, Radioisotopes & Reactors, Faculty of Applied Sciences, Delft University of Technology, Mekelweg 15, 2629JB, Delft, The Netherlands, (b)Laboratory of Physics, Helsinki University of Technology, P.O. Box 1100, 02015 HUT, Finland

Vacancy-impurity pairs (E centers) have an important role in the diffusion and electrical activation of donor impurity atoms. They are also fundamentally significant as basic objects to study the vacancy-impurity interaction. In this work we apply positron annihilation spectroscopy to study the atomic and electronic structures of V-P and V-P-Ge complexes in 2 MeV proton irradiated P-doped Si(0.96)Ge(0.04) strained samples on Si(100). We use a high-intensity positron beam and the two-dimensional detection of positron annihilation radiation (2D-ACAR) in order to obtain a much higher precision than in the more conventional Doppler broadening studies. The irradiation at 300 K is shown to create mostly V-P pairs, which are not neighbored by Ge atoms. The lack of anisotropy of the 2D-ACAR spectra indicates that the V-P pair does not prefer a certain lattice orientation in the strained samples. The 2D-ACAR experiments confirm the picture that the migration of V-P pairs at 450 K leads to the formation of V-P-Ge complexes, which have higher thermal stability [1]. By comparing the 2D-ACAR spectra of V-P and V-P-Ge defects we can extract the two-dimensional contribution of the Ge atom to the electronic structure of the E center. It is found to be isotropic for both 4s and 4p valence electrons as well as for the 3d core electrons of the Ge atom. We conclude that both P and Ge atoms occupy a random lattice site in the shell neighboring the vacancy, and no electronic or atomic relaxation due to the strain is observed within the accuracy of the 2D-ACAR.

[1] S.-L. Sihto, J. Slotte, J. Lento, K. Saarinen, E. V. Monakhov, A. Yu. Kuznetsov, and B. G. Svensson, Phys. Rev. B 68, 115307 (2003).

D/PII.15 LOW TEMPERATURE SOLID-PHASE EPITAXIAL REGROWTH OF AMORPHISED SILICON: A COMPARISON BETWEEN X-RAY MEASUREMENTS AND MEDIUM ENERGY ION SCATTERING

L. Capello, T.H. Metzger, E.S.R.F., BP 220, Grenoble, 38043, France, M. Werner, J.A. van den Berg, Joule Physics Lab., IMR, University of Salford, Salford M5 4WT, U.K., T. Feudel, M. Herden, AMD Saxony LLC & Co. KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Germany

Solid–Phase Epitaxial Regrowth (SPER) is considered as a potential solution to meet the specifications for ultra-shallow junctions in the 65 and 45nm technology nodes [1]. A batch of Epi-Si samples amorphised in the near-surface layers by As implantation, was produced to investigate the lattice recovery during SPER and the simultaneous evolution of defects. Annealing temperatures (550 °C – 700 °C) and times (200-10s) were used to characterize the stages of SPER along with the onset of defect annealing. In this work a comparison between medium energy ion scattering (MEIS) and synchrotron-based x-ray scattering results will be presented showing clear layer-by-layer regrowth, dopant atoms taking substitutional positions, and dopant segregation close to the surface. It is demonstrated that the complementary information the two techniques provide, are beneficial to both.

The same experimental approach was used to investigate the influence of the pre-amorphising implant using heavy ions on As-implanted Si, with particular interest in the near-surface region of the implant. This research was supported by EU grant IMPULSE: IST-2001-320061. Reference: 1 http://public.itrs.net

D/PII.16 **D-XII.02**

D/PII.17 CHARACTERIZATION OF ION-INDUCED AMORPHIZATION OF GAAS AND INAS USING PAC SPECTROSCOPY

R. Dogra(a,b), A.P. Byrne(b,c) and M.C. Ridgway(a), (a)Department of Electronic Materials Engineering, Research School of Physical Sciences and Engineering, Australian National University, ACT, Australia, (b)Department of Nuclear Physics, RSPhysSE, Australian National University, ACT, Australia, (c)Department of Physics, Faculty of Science, Australian National University, ACT, Australia

The III-V compound semiconductors have generated a considerable interest because of their technological importance. In order to exploit the full potential of these materials, doping with different ions is required. Ion implantation is the most attractive method of dopant incorporation for device fabrication because concentration of the dopants can be controlled precisely and almost all the elements can be implanted. The process of ion implantation is always accompanied by the radiation damage of the lattice and for higher doses, it leads to amorphisation. The perturbed angular correlation technique (PAC), based on nuclear hyperfine methods, has been utilized to understand the production and nature of the implantation induced crystalline to amorphous transformation in GaAs and InAs. The PAC spectroscopy, offers a high degree of sensitivity to local structural variations in the crystal lattice, requires introduction of radioactive probe nuclei in host material. The radioactive probe nuclei 111In were first introduced in the crystal lattice followed by implantation with stable Ge ions. The dose dependent crystalline, disordered and amorphous probe environments were identified from the measurement. The PAC results are interpreted in terms of direct amorphisation, overlap and composite models.

D/PII.18 POINT DEFECTS INTERACTION WITH EXTENDED DEFECTS AND IMPURITIES IN THE SI-SI-SIO2 SYSTEM DURING THE PROCESS OF ITS FORMATION

D. Kropman, Maritime Academy, Tallinn, Estonia, U. Abru, Tondi Electronics, Tallinn, Estonia, T. Kärner, Institute of Physics, Tartu University, Tartu, Estonia, Ü. Ugaste, Pedagogical University, Tallinn, Estonia, E. Mellikov, M. Kauk, Technical University, Tallinn, Estonia, I. Heinmaa, A. Samoson, Institute of Chemical Physics and Biophysics, Tallinn, Estonia

It has been shown that the vacancies type defects electron paramagnetic resonance (EPR) signal intensity dependence on the oxidation time is non-monotonous. This indicates that interaction between point defects, extended defects and impurities occurs in the Si-SiO2 system during the process of its formation. In the present work it has been established that EPR signal intensity dependencies on the oxide thickness reveal a minimum or a maximum depending on the oxidation ambient (impurity content).We suggest that the decrease of the EPR signal indicates the interaction between vacancies and interstitial Si atoms (or its complexes) at the interface, whereas the increase of this signal indicates that interstitial atoms and vacancies are separated and interaction between them is absent. The effective charge of SiO2 does not depend on the oxide thickness if an interaction between the point defects at the interface occurs, while if it is absent, the effective charge decreases with the oxide thickness, due to compensation of the positive SiO2 charge by negatively charged acceptor centres at the interface. It has been established that the differences between the dependence of the charge in SiO2 on the oxidation time in MOS structures prepared on n- and p-type wafers grown by CZ and FZ methods, respectively, coinside with the differences between charge in SiO2 revealed in samples oxidized in different ambient. The 1H NMR line width of the n-type samples is remarkably broader than that of the p-type samples. The extent of this effect goes up with the

extent to which the movement of adsorbed molecules is hindered by the strength of the magnetic interaction with the paramagnetic impurities of the adsorbent.

D/PII.19 STRUCTURAL CHARACTERISATION OF SELF-IMPLANTED Si AFTER HT-HP TREATMENT

W. Rzodkiewicz, A. Kudla and A. Misiuk, Institute of Electron Technology, Al. Lotników 46, 02-668 Warsaw, Poland

Healing of damages in implanted silicon is still not fully understood. Self-implanted silicon Si:Si is a model material in this research; the implantation-damaged area in Si:Si is under high quasi-hydrostatic stress, so application of external hydrostatic pressure (HP) at annealing of Si:Si makes it possible to obtain valuable information on the stress-related effects during out-annealing of structural damages.

Cz-Si-samples were subjected to the implantation with Si+ at 160 keV energy to a dose D=5x1016cm-2. Si:Si samples were treated at a high temperature (up to 1130oC) under hydrostatic argon pressure (up to 1.1 GPa) for 5h. In our investigations, spectroscopic ellipsometry (SE), X-Ray reciprocal space mapping (XRMS), and photoluminescence (PL) methods were applied. Changes in the dielectric function ε in both the as-implanted and HT-HP treated silicon samples has been determined by spectroscopic ellipsometry method. The considerable improvement of both optical and structural properties of the self-implanted silicon samples for such treatment conditions like p=1.1GPa, T=800oC, t=5h; has been observed. In the samples treated at temperature of 1000oC, for 5h, with the increase of pressure, the decrease of ε1 and ε2 in UV range has been observed. For samples treated under 1.1 GPa and for 5h, both ε1 and ε2 decreased with the increase of temperature in all spectra range. The correlation between results obtained by SE and other techniques is discussed.

D/PII.20 DIFFERENTIAL HALL PROFILING OF ULTRA-SHALLOW JUNCTIONS IN SI AND SOI

N.S. Bennett, A.J. Smith, B. Colombeau, R. Gwilliam, N.E.B. Cowern and B.J. Sealy, Advanced Technology Institute, University of Surrey, Guildford, Surrey GU2 7XH, U.K.

Determining the electrical characteristics of doped layers is a key challenge in understanding the success of the ion implantation and an anneal process. Hall measurements have the ability to measure the electrical activation and the carrier mobility. Differential Hall Measurement (DHM) is one method capable of determining these electrical properties as a function of depth. Unlike Spreading Resistance Profiling (SRP), this technique can measure the active carrier profile without any assumption on the magnitude of the mobility.

In this paper, we demonstrate a reproducible DHM technique to profile ultra-shallow junctions down to 15nm using a novel native oxide removal process. This technique is shown to profile p and n type layers with a depth resolution of 1-2nm. Comparisons with atomic profiles measured by Secondary Ion Mass Spectrometry demonstrate the accuracy and advantages of the DHM profiles. Results for mobility values as a function of carrier concentration for different experimental conditions provide an important data for accurate modelling of junction behaviour. Finally, we shall show how to optimise the technique parameters to overcome some of the inherent difficulties that are associated with DHM profiling such as layer removal uniformity, profile distortion due to surface states, and limited depth resolution.

D/PII.21 HIGH DEPTH RESOLUTION PROFILING OF THE DAMAGE ANNEALING AND DOPANT REDISTRIBUTION OF ULTRA SHALLOW As IMPLANTS IN PRE-AMORPHISED Si AND SOI

M. Werner, J.A. van den Berg, M.A. Reading and D.G. Armour, Joule Physics Laboratory, Institute of Materials Research, University of Salford, Salford M5 4WT, U.K., T. Feudel and M. Herden, AMD Saxony LLC & Co. KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Germany, M. Bersani and D. Giubertoni, ITC IRST, 38050 Povo - Trento, Italy, P. Bailey and T.C.Q. Noakes, CCLRC Daresbury Laboratory, Daresbury WA4 4A, U.K.

Medium energy ion scattering (MEIS) and secondary ion mass spectrometry (SIMS) have been used to characterise the damage annealing and dopant redistribution of ultra shallow As implants as a function of anneal temperature and substrate type i.e. bulk Cz Si, epi Si, 60 and 100 nm SOI. As implants were performed at 2.5 and 3 keV into crystalline and pre-amorphised samples. For bulk Si samples upon annealing to temperatures between 550-700 ˚C, MEIS showed the movement of a sharp amorphous/crystalline interface characteristic of solid phase epitaxial regrowth (SPER). At 700 ˚C nearly half of the As dopant had moved into substitutional sites; the remainder was snowploughed in front of the advancing interface. forming a < 1 nm wide, As rich layer, clearly trapped under the oxide. Ultra low energy SIMS profiling showed good agreement with MEIS results, and confirmed that As retention was complete following annealing in a N2/ 6% O2 ambient.

Unlike for bulk Si, MEIS shows that the interface for the Si regrowth in SOI, pre-amorphised with 40 keV Xe bombardment is broad. It is clearly not layer by layer, neither for the 60 nm SOI for which, according to SRIM calculations, some of the Xe and Si recoils reached the buried Si/ oxide interface, nor for the 100 nm PAI where this is not the case. The large width of the amorphous crystalline interface observed, indicates the formation of an irregular interface, which it is suggested is due to the localised trapping of migrating Si interstitials into amorphous humps for both the 60 and the 100 nm SOI.

D/PII.22 DOSE CHARACTERIZATION OF LOW ENERGY ARSENIC IMPLANTS USING NAA, SIMS AND TXRF

Amiya R. Ghatak-Roy, Technos Interntional, Tempe AZ 85283, USA, Latha Vasudevan, Texas A&M University, College Station TX 77843-3575, USA, Majeed A. Foad, Applied Materials Inc., Sunnyvale CA 94086, USA

The trend in semiconductor industries is towards low energy implants. This is necessitated by ever shrinking geometry for leading edge technologies. For advanced source / drain extension, ion energies are now approaching 1 keV in production. At this low energy, various factors become important in that the implant dose requirement is stringent, as it affects both the electrically active concentration and the junction depth. As a result, metrology for dose measurement has become very important. So far SIMS, the workhorse for implant dose measurement, has been keeping pace with the lowering of implant energy. However, for arsenic around 2 keV, SIMS may show some shortcomings for analysis due to initial surface sputtering and subsequent matrix effects.

Various technologies are being evaluated currently. X-ray based technology has been a contender as a fast and non destructive technique. In the present work we characterized the low energy Arsenic dose measurement by Total-Reflection X-Ray Fluorescence (TXRF) and SIMS and compare the results with those obtained by Neutron Activation Analysis (NAA). The latter measurement was calibrated using a NIST standard. Excellent correlation for low energy Arsenic implant dose measurement has been found among TXRF, SIMS and NAA.

D/PII.23 EVALUATION OF SCANNING SCHOTTKY CAPACITANCE MICROSCOPY FOR THE CHARACTERISATION OF DOPING PROFILES

D. Goghero, B. Gautier, A. Descamps, G. Bremond, Laboratoire de Physique de la Matière (UMR-CNRS 5511), 7 Avenue Capelle, 69621 Villeurbanne Cedex, France

The Scanning Capacitance Microscopy is a widely used method for the characterisation of doping profiles in the structures of the microelectronics industry. Because of it is relatively easy to implement, and because it is able to discriminate between n-type and p-type dopants, SCM has demonstrated its capabitilities to be a valuable tool for device failure check. However, the future devices require a nanometric resolution and precise quantification of the dopant concentration, and SCM still lacks reproducibility and spatial resolution compared to other methods like Scanning Spreading Resistance Microscopy (SSRM).

One of the main problems which hampers the reproducibility of the SCM measurements is the quality of the oxide. We aim in this paper to evaluate the performances of a detection method, the Scanning Schottky Capacitance Microscopy (SSCM), which suppresses the oxide involved in the SCM. Test samples (delta-doped layers and staircases) are used to characterise the spatial resolution, the reproducibility and the capabiblities in terms of quantification of this method.

D/PII.24 QUALITATIVE CHARACTERIZATION OF SONOS TRANSISTOR UTILIZING SCANNING CAPACITANCE MICROSCOPE(SCM) AND SCANNIING SPREAD RESISTANCE MICROSCOPE(SSRM)

Jinhee Heo(a), Deoksu Kim(a), Chungwoo Kim(b), Ilsub Chung(a), (a)SungKyunKwan University, Chunchun-Dong, Jangan-Ku, Suwon, Korea, (b)Samsung Advanced Institute of Technology, MD Laboratory, P.O. Box 111, Suwon, Korea

Continuous shrinkage in the memory devices demands further understanding at shallow junction and channel region. Scanning Capacitance Microscope (SCM) and Scanning Spread Resistance microscope (SSRM) can provide reliable information about the electrical and physical junction structure simultaneously. In this work, we attempted to visualize the difference in the doping concentration of split-gate structure SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) transistor with thin Oxide-Nitride-Oxide (2.3/6/4.5nm). From SCM image, we could identify the source and drain region with different doping concentration from channel region. In addition, we could identify a gate oxide layer and a depletion region. We could obtain similar results from SSRM. However, SSRM shows a better resolution for highly doped region. For this experiment, the cross-sectional sample has been prepared using FIB and hand-polishing method. The results show SCM and SSRM are very useful method to analyze the doping profile hear the junction as well as channel.

D/PII.25 ALL ELECTRICAL RESISTIVITY PROFILING TECHNIQUE FOR ION IMPLANTED SEMICONDUCTOR MATERIALS

Santolo Daliento, Luigi Mele, Paolo Spirito, University of Naples "Federico II", Department of Electronic Engineerig & TLC, Via Claudio 21, 80125 Napoli, Italy

In this paper we propose an all electrical resistivity profiling technique specially suitable to analyse resistivity changes induced by light ion implantation used in lifetime tailoring processes. The technique is based on the operation of a test device formed by a surface diode, whose function is the injection of minority carriers into the layer under investigation, and a control electrode on the back. Minority carriers injected by the diode ca be confined at an arbitrary distance from the surface by applying a dc voltage on the back. By applying an incremental voltage ∆V to the back, the confine of minority carriers moves of ∆x toward the surface and an incremental diode current ∆I can be revealed. The ratio ∆V/∆I is directly related to the resistivity of the elemental ∆x. Two dimensional simulations have shown the capability of the technique to correctly reproduce sharply variable resistivity profiles. Also, experimental comparisons with spreading resistance profiles obtained on Helium implanted samples have shown an excellent agreement. The analysis of the resistivity profiles versus temperature has permitted to define the energy levels responsible for the resistivity variation.

D/PII.26 CARRIER RECOMBINATION VELOCITIES AT THE SiO2/Si INTERFACE INVESTIGATED BY A PHOTOTHERMAL MICROSCOPY

T. Ikari, A. Fukuyama, University of Miyazaki, T. Murata, M. Suemitsu, Tohoku University, Sendai, Japan and N. Haddad, V. Reita, J.P. Roger, D. Fournier, ESPCI, Paris, France

Demand for drastic decreasing of the oxide thickness in the MOS structure requires an improvement of the quality of both the oxide film itself and the interface with the substrate. This is because the SiO2/Si interface plays an important role when the oxide thickness becomes smaller. Photothermal microscopy has been developed for investigating carrier diffusivity, lifetime and surface recombination velocity in Si [1]. We present here the effect of the oxide thickness on the interface recombination velocity. SiO2 films were grown in the dry oxygen flowing furnace on the p- Si with thicknesses of 100 and 78 nm. Temperature rise due to photo excitation was measured in terms of a reflectivity as a function of distance from the pump beam. Curve fitting procedures with the theoretical prediction results in the estimation of the interface recombination velocity. The observed velocities are 300 and 200 cm/s for the sample with the thicknesses of 78 and 100 nm, respectively. This is smaller than 3000cm/s observed for the sample with a native oxide layer around a few nm. Thick oxide layer improves the quality of the SiO2/Si interface.

[1] T. Ikari, J. P. Roger and D. Fournier, Rev. Sci. Instruments, 74, 553 (2003).

D/PII.27 PHOTOELECTRICAL INVESTIGATION OF MOS STRUCTURES WITH OPTICALLY THICK AL AND POLY-SI GATES

A. Kudla, K. Piskorski, H.M. Przewlocki, Institute of Electron Technology, Al. Lotnikow 32/44, 02-668 Warsaw, Poland

The threshold voltage of modern transistors depends mostly on contact potential difference fMS. The fMS factor can be exactly determined with photoelectric method. Application of the UV laser, and proper shaping of the light beam, allows determination of the fMS factor with photoelectric method for structures with Al and poly-Si gates several hundreds nanometers thick.

MOS structures were formed on Si substrates;,<111> wafers were thermally oxidized to thicknesses from 10 to 60 nm. Al and poly-Si layers about 400nm thick were deposited and electrodes were formed by lithography. Structures with Al layer were annealed at 450C in forming gas atmosphere. For structures both with Al gate and poly-Si gate dark currents and photocurrents were measured showing good isolating properties. With UV light at l=244nm and P=10mW, and light spot d=20mm photocurrents were measured and the zero-photocurrent gate voltage VG0 (associated to the fMS factor) was (for the structures with poly-Si gate, for the first time) determined. The fMS lateral distribution is different for structures with Al and poly -Si gates. For structures with Al gate both flat band voltage VFB and the fMS factor depends on structure perimeter to area ratio. Such dependence is not

observed for structures with poly-Si gate. This difference can be explained by structural changes in SiO2 caused by Al electrodes.

D/PII.28 MOLECULAR DYNAMICS CHARACTERIZATION OF AS-IMPLANTED DAMAGE IN SILICON

Iván Santos, Luis A. Marqués, Lourdes Pelaz, Pedro López, María Aboy and Juan Barbolla, Dpto. de Electricidad y Electrónica, Universidad de Valladolid, E.T.S.I. Telecomunicaciones, Campus Miguel Delibes s/n, 47011, Spain

The use of SPEG of amorphous layers generated by ion implantation to achieve highly active and abrupt dopant profiles has revealed the need of predictive amorphization and recrystalization models. One of the difficulties for its development is the lack of an accurate description of the as-implanted damage. Models based on the binary collision approximation (BCA) or on the modified Kinchin-Pease formula provide acceptable ion profiles but only describe the damage in terms of Frenkel pairs, which is insufficient for detailed amorphization models. In turn, molecular dynamics (MD) simulations shows the formation of amorphous pockets and defect clusters during the implantation, in agreement with experiments. In this work we have characterized the morphology of the damage generated by several ions types in Si using MD techniques. We simulate hundreds of independent cascades for different ion types because a statistical study is needed to obtain representative results. In the case of Si implantation, we have observed that most of the damage is in the form of point defects or small defect clusters. About 0.5 % of the generated defects are agglomerates with more than 100 displaced atoms. We have found that small defects are interstitial rich, while big agglomerates have a deficit of atoms. These big defects or amorphous pockets are responsible for the amorphization process. The relation between our results and those predicted by the modified Kinchin-Pease formula and BCA will also be discussed.

D/PII.29 AB-INITIO STUDY OF THE EFFECT OF HYDROGEN AND POINT DEFECTS ON ARSENIC SEGREGATION AT Si(100)/SiO2 INTERFACES

Karthik Ravichandran and Wolfgang Windl, Department of Materials Science and Engineering, The Ohio State University, Columbus OH 43210-1178, USA

The previously suggested segregation model for arsenic at Si/SiO2 interfaces based on a combined trapping/pairing model [J. Dabrowski et al., Phys. Rev. B 65, 245305 (2002)] requires high binding energies for interface vacancies, which our results of ~0.2 eV cannot confirm. As an alternative explanation, we present ab-initio results which show that As and hydrogen bond with an energy gain of 1.5-3 eV with their minimum-energy position at the interface, which creates additional trapping sites for As segregation. The inclusion of hydrogen into the modeling might thus be able to explain the differences between the previous model and experiments.

D/PII.30 COMPREHENSIVE MODELING OF ION-IMPLANT AMORPHIZATION IN SILICON

K.R.C. Mok(a,b), M. Jaraiz(a), I. Martin-Bragado(a), J.E. Rubio(a), P. Castrillo(a), R. Pinacho(a), J. Barbolla(a), M.P. Srinivasan(a,b), (a)Dept. of Electronics, University of Valladolid. Campus Miguel Delibes. Camino del Cementerio S/N. 47011 Valladolid, Spain, (b)Dept. of Chemical and Biomolecular Engineering. National University of Singapore. 4 Engineering Drive 4, 117576 Singapore

A physically based damage accumulation model has been developed to simulate the ion-implant induced amorphization process in silicon. It has been implemented in an atomistic kinetic Monte Carlo simulator, and is suitable for device-sized process simulations. Based on damage structures known as amorphous pockets (AP), which are three-dimensional agglomerates of interstitials (I) and vacancies (V) surrounded by crystalline silicon, the model is able to reproduce a wide range of experimental observations of damage accumulation and amorphization with interdependent implantation parameters. Instead of recombining the I´s and V´s instantaneously, the AP recombination rate is a function of its effective size, defined as the minimum number of I´s or V´s it contains. The parameters used in the model were calibrated using experimental silicon amorphous-crystalline transition temperature as a function of dose rate for C, Si, Ar, Ge, Kr, Xe (12amu to 132 amu). In addition to obtaining good fits to this set of experiments, the model also correctly predicts the dose at which amorphization takes place by Ne and Sn, which were not used in the parameter extraction procedure. Furthermore, it reproduces the superlinear damage build-up with dose, extent of amorphous layer and the superadditivity effect, which results in greater amount of damage by implanting a given dose at a given dose rate using clusters instead of individual atoms.

D/PII.31 ION-IMPLANT SIMULATIONS: THE EFFECT OF DEFECT SPATIAL CORRELATION ON DAMAGE ACCUMULATION

K.R.C. Mok(a,b), M. Jaraiz(a), I. Martin-Bragado(a), J.E. Rubio(a), P. Castrillo(a), R. Pinacho(a), J. Barbolla(a), M.P. Srinivasan(a,b), (a)Dept. of Electronics, University of Valladolid, Campus Miguel Delibes, Camino del Cementerio S/N, 47011 Valladolid, Spain, (b)Dept. of Chemical and Biomolecular Engineering, National University of Singapore, 4 Engineering Drive 4, 117576 Singapore

A predictive damage accumulation model has been developed and implemented in a kinetic Monte Carlo simulator. The model assumes the amorphous pocket (AP) recombination rate to be a function of its effective size, defined as the minimum number of interstitials (I) and vacancies (V) it contains, regardless of their spatial configuration. AP´s are three-dimensional (3D) agglomerates of I´s and V´s, whose initial coordinates are generated by a binary collision approximation (BCA) code. Alternatively, the initial coordinates of the I´s and V´s could be randomly generated from the concentration distribution of an input damage profile. This work addresses the importance of the spatial correlation of I´s and V´s in modeling damage accumulation and amorphization. Low temperature implantations were simulated to avoid dynamic annealing in order to compare the initial damage morphology. For the same damage level, implant simulation by BCA resulted in lighter implant ions having smaller AP´s sizes, implying more dilute damage compared to heavier ions. The role of the cascade structure was studied by loading the same damage profile and randomly generating the damage. In this case, the resulting damage was even more dilute than that of the light ions. Therefore, the 3D cascade configuration is necessary to model damage accumulation accurately.

D/PII.32 FORMATION OF HIGHLY MOBILE DI-INTERSTITIALS DURING ION IMPLANTATION

M. Posselt, Forschungszentrum Rossendorf, Institute of Ion Beam Physics and Materials Research, P.O. Box 510119, 01314 Dresden, Germany

The formation of di-interstitials in silicon during ion bombardment and their migration are studied by atomistic computer simulations. A recently developed combination of time-ordered simulations based on the binary collision approximation with classical molecular dynamics (MD) calculations is employed in order to treat the ballistic processes and the subsequent fast relaxation which occur immediately after ion impact. The metastable defect structure formed after the fast relaxation has been completed does not only consist of isolated mono-vacancies and mono-interstitials but also of more complex defects. Amongst the different defect species a small percentage of di-interstitials is found. Their properties are investigated in more detail using classical MD simulations. The results

on the structure and energetics of di-interstitials are compared with literature data. The di-interstitial migration is investigated for temperatures between 600 and 1600 K. The di-interstitial diffusivity and the self-diffusion coefficient per defect are calculated. It is found that the di-interstitial is highly mobile. The migration mechanism shows a pronounced dependence on the temperature. The elementary mechanisms of di-interstitial migration are investigated by the visual analysis of movies and snapshots of the atomic rearrangements. The present results are compared with the few literature data on di-interstitial diffusion. The high mobility of the di-interstitials and the fact that they can be already formed during the ion implantation may have implications for the current understanding of the results of many experimental investigations performed in the last decade, in particular for the explanation of the implantation-induced migration of interstitial-like defects at room temperature.

D/PII.33 ATOMISTIC STUDY OF INTRINSIC DEFECTS IN GERMANIUM

H. Gessner, M. Posselt, Forschungszentrum Rossendorf, Institute of Ion Beam Physics and Materials Research, P.O. Box 510119, 01314 Dresden, Germany

The formation of di-interstitials in silicon during ion bombardment and their migration are studied by atomistic computer simulations. A recently developed combination of time-ordered simulations based on the binary collision approximation with classical molecular dynamics (MD) calculations is employed in order to treat the ballistic processes and the subsequent fast relaxation which occur immediately after ion impact. The metastable defect structure formed after the fast relaxation has been completed does not only consist of isolated mono-vacancies and mono-interstitials but also of more complex defects. Amongst the different defect species a small percentage of di-interstitials is found. Their properties are investigated in more detail using classical MD simulations. The results on the structure and energetics of di-interstitials are compared with literature data. The di-interstitial migration is investigated for temperatures between 600 and 1600 K. The di-interstitial diffusivity and the self-diffusion coefficient per defect are calculated. It is found that the di-interstitial is highly mobile. The migration mechanism shows a pronounced dependence on the temperature. The elementary mechanisms of di-interstitial migration are investigated by the visual analysis of movies and snapshots of the atomic rearrangements. The present results are compared with the few literature data on di-interstitial diffusion. The high mobility of the di-interstitials and the fact that they can be already formed during the ion implantation may have implications for the current understanding of the results of many experimental investigations performed in the last decade, in particular for the explanation of the implantation-induced migration of interstitial-like defects at room temperature.

D/PII.34 BIMODAL DISTRIBUTION OF DAMAGE MORPHOLOGY GENERATED BY ION IMPLANTATION

I. Martin-Bragado(a), K.R.C. Mok(a,b), M. Jaraiz(a), E. Rubio(a), P. Castrillo(a), R. Pinacho (a), J. Barbolla(a), (a)Dept. of Electronics, University of Valladolid, Campus Miguel Delibes, Camino del Cementerio S/N, 47011 Valladolid, Spain, (b)Department of Chemical Engineering, National University of Singapore, 4 Engineering Drive 4, 117576 Singapore

In this work we use a recently developed nucleation and evolution model of damage based on amorphous pockets (APs) that has been implemented in an atomistic Kinetic Monte Carlo simulator. In the model APs are disordered structures (InVm) which agglomerate interstititials (I) and vacancies (V) and recombine them with a thermal energy that only depend on the AP effective size (min(n,m)). This model has been used to study the size distribution of APs during different ion implantations. Depending strongly on the dose rate, ion mass and temperature the APs can evolve to a similar number of Is and Vs (n  m) distribution, to Is (m0) or Vs (n0) clusters or to a mixture of both. This behavior corresponds to a bimodal (APs/clusters) distribution of damage. The consequences of these different distributions are also studied, in particular how subsequent annelings will lead to different results dpending on the damage morphology, due to the different thermal behavior of clusters, which are more difficult to dissolve than APs. We show that the same damage concentration obtained through different implant conditions has a different morphology and, consecuently, exhibit a different annealing behavior.

D/PII.35 TECHNOLOGY CAD OF SILICIDED CONTACT FOR ELEVATED SOURCE DRAIN ENGINEERING

A.R. Saha and C.K. Maiti, Department of Electronics & ECE, Indian Institute of Technology, Kharagpur 721302, India

Increased functionality at low cost needs an excessively high package density of CMOS VLSI chips, leading to aggressive scaling of the MOSFETs.The saturation drain current, which depends on contact potential and resistivity of scaled device being the most important parameter for the speed of operation of MOSFETs.In this context a silicided Schottky barrier may realized as an elevated source drain structure. Silicided MOSFETs have recently been proposed as candidates for the sub 0.1 μm regimes due to their ease of manufacture and other advantages over conventional CMOS devices.In this paper,for the first time, we show the enhanced device characteristics of a symmetrical silicided SB-MOSFET (Schottky Barrier) using 2D device simulator.Numerical simulation based on Silvaco-ATLAS and ATHENA is used to explore the processing and design parameter space for silicided SB-MOSFETs.In simulation various material parameter for silicide, Si and relaxed SiGe have been incorporated through the C-interpreter function.The extracted sheet resistivity as a function of annealing temperature of a silicided source drain contact is found to be lower than the conventional ohmic contacts and interconnects. Simulated results indicate that the higher sub-threshold slope for silicided SB-MOSFET,compared to controlled silicon device may be due to the higher interface states in the alloyed interface.But one important aspect is that the elevated source drain with silicide structure effectively reduces the contact and parasitic series resistance between source and drain.In conclusion,the design and simulation of high performance silicided MOSFETs are presented.The advantages to be gained by using silicide contacts in conventional Si-CMOS technology have been examined through simulation.

D/PII.36 AN INVESTIGATION ON THE MODELING OF BED AND TED OF ULTRALOW ENERGY IMPLANTED BORON IN SILICON

J. Marcon, L. Ihaddadene-Lecoq, K. Masmoudi and K. Ketata, Laboratory of Electronic Microtechnology and Instrumentation (LEMI), University of Rouen, 76821 Mont Saint Aignan, France

The simulation of Boride Enhanced Diffusion and Transient Enhanced Diffusion is a key challenge for the modelling and the realization of future integrated circuits. During the post-implantation annealing, the BED and TED of B occur and it may increase the junction depth. In addition, high-concentration B will lead to B clustering and B precipitation, which reduce electrical activation. These phenomena make the diffusion simulation of ultra-low-energy-implanted B difficult, and to the author’s knowledge, there have been no simulation studies that fully take all of these phenomena into account for low energy BF2 implantation. In our study, low energy BF2 (2 keV) and dose of 1x1015 cm-2 have been used. RTA were carried out at 950, 1000, 1050 and 1100 °C. Following Uematsu’s works, the simulations satisfactory reproduce the SIMS experimental profiles. The effect of fluorine on boron diffusion has been discussed. The simulated parameters of BED/TED effects and Type

I default (extrinsic dislocation loops located around the projected range) have been discussed. We have considered the possible formation of fluorine clusters which involves interstitial boron.

D/PII.37 ANALYTIC MODEL FOR ION CHANNELING IN SUCCESSIVE IMPLANTATIONS IN CRYSTALLINE SILICON

S. Strauss, C. Zechner, A. Terterian, R. Gautschi, A. Erlebach and A. Scholze

Successive ion implantations are frequently used in the fabrication of silicon devices. Each ion implantation increases the crystal damage in the region near the surface. For successive implantations, the ion channeling in perfect crystal channels is reduced and the channeling tail is lowered. In the process simulation, the impurity distribution after ion implantation is often calculated as the sum of two Pearson functions, of which the second covers the channeling ions. In this work, we present a general model for the reduction of channeling in successive implantations. The crystal damage from the implantations is monitored and used for the calculation of a differential channel dose. The model allows a fast analytic calculation of impurity profiles in 1D, 2D, and 3D process simulators. It provides similar accuracy as Monte Carlo simulations and gives excellent agreement with SIMS data of successive ion implantations.

D/PII.38 LOCAL VIBRATIONS ON HYDROGEN DIMERS IN DILUTE SIGE CRYSTALLINE SOLUTIONS

J. Coutinho and V.J.B. Torres, Department of Physics, University of Aveiro, Campus Santiago, 3810-193 Aveiro, Portugal, R.N. Pereira, Institut for Fysik og Astronomi, Århus Universitet, 8000 Århus, Denmark, S. Öberg, Department of Mathematics, Luleå University of Technology, Luleå 97187, Sweden and P.R. Briddon, School of Natural Sciences, University of Newcastle upon Tyne, Newcastle upon Tyne NE1 7RU, U.K.

Atomic hydrogen is a concomitant impurity in semiconductors. Its presence in Si, Ge and SiGe alloys has been established by means of paramagnetic resonance, optical, electrical and theoretical modeling studies. Hydrogen self-trapping is known to occur in Si and Ge, resulting in the formation of molecular hydrogen and H2* interstitial dimers. Here we report on the properties of H2*complexes in dilute SiGe alloys, by using an ab-initio density functional method. It is found that these complexes form preferentially within Si-rich regions. H2* dimers in Si-rich alloys show vibrational properties similar to those in pure Si. On the other hand, in Ge-rich material the minority Si atoms act as nucleation sites, with the consequent formation of at least one preferential H2*-Si complex variant showing a distinct vibrational activity.

D/PII.39 AB-INITIO STUDY OF THE INTERFACE BETWEEN Si(100) AND CRYSTALLINE LANTHANUM ALUMINIUM OXIDE

Dipanjan Sen and Wolfgang Windl, Dept. of Materials Science and Engineering, The Ohio State University, Columbus OH, USA

One of the crucial needs in the semiconductor industry is the development of high-K dielectric materials as gate dielectrics in transistors to control tunneling current leakage between gate and channel. A prime requirement is that the material should form a smooth defect free interface with silicon. In this presentation, we study the interface of Si(100) with crystalline lanthanum aluminium oxide (LAO) using ab-initio calculations to determine and understand the thermodynamically favored interface structure. To account for non-stoichiometric interfaces, we have improved previous work and present a universally applicable method to calculate interfacial free energies that allows an energy comparison between stoichiometrically non-equivalent structures. Our theoretical results are in agreement with the electron-microscope measuerement and find that the interface structure with the lowest energy possesses a non-stoichiometric LaO layer interface layer which results in a charge-neutral system with interesting ordering effects.

D/PII.40 TIGHT-BINDING MOLECULAR DYNAMICS SIMULATION OF BORON DIFFUSION IN SILICON

V. Cuny and E. Lampin, IEMN, Avenue Poincaré, 59654 Villeneuve d'Ascq Cedex, France

The aim of this work is to develop atomistic simulations of the diffusion of dopants in situations where the classical continuous models failed or must be enriched. We have choosen the technique of molecular dynamics which is adapted to the ultrafast phenomena such as laser annealing or the 'complex' materials such as SiGe alloys. The tight-binding frame of the molecular dynamics method was chosen because it is based on the calculation of the electronic structure of the system and it is therefore more precise than the methods using classical potentials. This method is however faster than the ab initio methods because the elements of the Hamiltonian matrix are described by a whole set of parametrized functions. Moreover the method allows to calculate the properties of systems with more atoms. We will present on this poster the first results on the boron diffusion with the tight-binding molecular dynamics method and the coupling of these results with those coming from the state of the art of atomic scale calculations. These data will be injected in the classical process simulator FLOOPS and applied to the realization of ultrashallow junctions.

D/PII.41 DYNAMICS AND ENERGETICS OF SI(100) SURFACE RECONSTRUCTION

C.S. Guo, R.Q. Zhang, Center of Super-Diamond and Advanced Films & Department of Physics and Materials Science, City University Hong Kong, Hong Kong SAR

Si(100) surface is important because most silicon devices are formed on it. We researched this surface with density functional theory (DFT) and found that its reconstructions are very sensitive to initiatory morphology of the top atomic layer. The result indicates that Si(100) surface may involve domains of different geometries reconstructed from various possible starting local surface structures affected by temperature fluctuation. Our additional study on the stability of the reconstructed surface showed that the reconstructions are also sensitive to external disturbances caused by possible measurements in experiments using STM and AFM. Our results indicate that temperature and tip-surface interactions will lead to transformation of reconstructed configuration between multiple states of this surface.

D/PII.42 SIMULATIONS OF ARSENIC AND BORON CO-IMPLANTED IN SILICON DURING R.T.A. FOR ULTRA-SHALLOW JUNCTIONS REALIZATION

A. Merabet, Laboratoire Physique et Mécanique des Matériaux Métalliques, O.M.P., Faculté des Sciences de l'Ingénieur, Université de Sétif, Sétif 19000, Algérie

The ionic implantation techniques are commonly used in the ULSI area. They permit the redistribution of impurities in depth with accuracy. The formation of thin junctions is realised by arsenic (1016 at.cm-2; 100 KeV) preamorphisation of substrate, followed by the boron (2x1015 at.cm-2; 30 KeV) implantation. After that, we carry out a rapid thermal annealing for 20s at temperatures ranging from 1000 to 1150°C which permits to obtain simultaneous the recrystallisation of the initial amorphous layer and the activation of impurities. We have used the simulator of TITAN process in the version V developed in CNS (CNET, Meylan) and installed in CIMIRLY (Lyon-France). It permits a two-dimensional simulation. This simulator uses the finished elements method for the

resolution equations of codiffusion. We have simulated the codiffusion profiles of arsenic and boron into the silicon using the parameters by defect of the simulator. We have noted the difference between the experimental distribution profiles measured with Secondary Ion Mass Spectrometry (SIMS) and those calculated. This leads us to adjust the profiles, changing the diffusion coefficient of dopant in order to obtain the simulated profiles corresponding in a better way to the experimental profiles. The arsenic diffusivity values vary from 2x10-13 (1000°C) to 2x10-12 (1150°C) cm2/s in the amorphised zone ; and from 4x10-16 (1000°C) to 6x10-14 (1150°C) cm2/s in the crystalline zone. As for as boron is concerned, they are from 10-15 (1000°C) to 6x10-14 (1150°C) cm2/s; and from 10-14 (1000°C) to 4x10-13 (1150°C) cm2/s in the two zones respectively cited.

D/PII.43 CONTROL OF SI NANOCRYSTALS FABRICATED BY ULTRA-LOW ENERGY ION IMPLANTATION FOR NON VOLATILE MEMORIES

H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, M. Carrada, G. Ben Assayag, A. Claverie, CEMES-CNRS, 29 rue J. Marvig, 31055 Toulouse, France, P. Dimitrakis, P. Normand, IMEL, 'Demokritos', 15310 Aghia Praskevi, Greece, M. Perego, M. Fanciulli, MDM-INFM, Via Olivetti 2, Agrate Brianza, Italy

Performance and scalability of non-volatile memories can be improved by new devices based on Multi-dot Floating Gate MOSFETs where Si nanocrystals (ncs) embedded in a thin oxide are the charge storage elements. We show here how to manipulate the depth-position, size and surface density of 2D arrays of Si ncs embedded in thin (<10 nm) SiO2 layers, fabricated by ultra-low energy (≤1 keV) ion implantation and subsequent annealing. Particular emphasis is focused upon the influence of implantation and annealing conditions on the ncs characteristics and the charge storage properties of associated MOS structures. Specific experimental methods have been developed to characterize these populations including Fresnel imaging for distance measurements, Energy Filtered imaging to measure ncs size and density and TOF-SIMS to measure the depth-distribution of excess Si in the oxide. Annealing under oxidizing ambient has been found essential for the optimization of the memory properties as charge storage at low gate voltages and enhanced charge retention times are obtained. The evolution of the ncs population has been studied as a function of the oxidation conditions under N2+O2. A Deal-Grove model extended to spherical shape has been carried out for the self-limiting oxidation of embedded Si ncs. The model predictions are in good agreement with the experimental results.

D/PII.44 STUDY OF THE UNIPOLAR BIAS RECHARGING PHENOMENON IN THE NONVOLATILE MEMORY CELLS CONTAINING SILICON NANODOTS

V. Turchanikov, A. Nazarov, V. Lysenko, Lashkarev Inst. of Semiconductor Physics, NANU, Kyiv, Ukraine, O. Winkler, B. Spangenberg, H. Kurz, Inst. of Semiconductor Electronics, Aachen University, Aachen, Germany

We studied the formation kinetics of write/erase window in nonvolatile memory (NVM) Metal-Oxide-Silicon (MOS) cells containing silicon nanodots inside the dielectric. With this goal we carried out relaxation measurements of the MOS capacitor’s flatband voltage shift during the application of bias pulses of different durations, amplitudes and polarities. These cells were formed by LPCVD 5-10 nm Si-nanodots deposition on thin (2-3 nm) SiO2 with subsequent thick (50 nm) silicon dioxide layer deposition by RPECVD and Al metallization.

It is well known that for the formation of write/erase window a different polarity bias pulse must be applied to the NVM cell. As a rule, bias stressing (BS) with positive potential on the metal leads to electrons trapping or holes emission and negative potential leads to the holes trapping or electrons emission in nanodots. This was the case in our structures biased by +27 V and -36 V gate potentials with window width of 1.25 V. But if we change BS window potentials to +27 V and +36 V we also observed window formation with width of 1.5 V under the unipolar bias. Moreover, under +36 V biasing positive charge accumulation instead of its dissipation was observed. This phenomenon is discussed on the basis of charge trapping in dielectric, nanodots and nanodots ionization processes. Additional experiments prove that the main source of positive charge accumulation is the process of nanodots ionization under BS.

D/PII.45 CHARACTERIZATION OF PROGRAM AND ERASE PROPERTIES USIING FOWLER-NORDHEIM TUNNELING IN THE 30NM SILICON-OXIDE-NITRIDE-OXIDE-SILICON NON-VOLATILE MEMORIES

Ho chan Ham(a), Jin hee Heo(a), Chung woo Kim(b), Ilsub Chung(a) (a)SungKyunKwan University, (b)Samsung Advanced Institute of Technology

The program and erase properties of 30 nm Silicon-Oxide-Nitride-Oxide-Silicon transistors with thin Oxide-Nitride-Oxide thickness 2.3/6/4.5nm are evaluated as a function of a pulse width and a gate bias voltage. SONOS transistor was fabricated utilizing side wall patterning technique on SOI substrate. We characterized electrical properties based on Fowler-Nordheim tunneling method. Under the program / erase condition like 11V/100ms and -11V/100ms, we observed that program and erase threshold window appears as 2V, 2.35V respectively with changing gate bias voltage. On the other hand, in the pulse mode, we found that the threshold windows were 2.3V, 2.5V, respectively. As for the retention characteristic, the threshold window was kept in 2.44V at the room temperature after 10000 sec. However, the threshold window was predicted to decrease to 1.45 V after 10 years. In addition, the endurance property in terms of the initial memory window was maintained until 10,000 cycles of program / erase without ant change.

D/PII.46 DETERMINATIONS AND CONTROLS OF THE MEMORY TRAP IN OXIDE-NITRIDE-OXIDE (ONO) STRUCTURES

C.J. Park(a), J.S. Oh(a), Y.H. Lee(a) , W.C. Yang(a), H.Y. Cho(a), J.H. Han(b) and J.W. Kim(b), (a)Quantum-functional Semiconductor Research Center and Dept. of Physics, Dongguk University, Seoul 100-715, Korea, (b)Devices Lab, Samsung Advanced Institute of Technology, Kiheung-eup Yongin-city Kyunggi-do 449-701, Korea

Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) structures which have various deep traps in the layers have been highlighted on next non-volatile memory devices. SONOS structures have been fabricated on p-type and n-type silicon substrates that consist of blocking oxide 8 nm silicon nitride 6 nm, and tunneling oxide 2 nm, respectively. In ONO structures with and nitride layers, traps distribution and energies distribution have been investigated by using Current-voltage (IV), Capacitance-voltage (CV), Deep level transient spectroscopy (DLTS), Current deep level transient spectroscopy (C-DLTS), Thermally Stimulated Current (TSC), and Thermally stimulated capacitance (TSCAP) measurements. The hole traps are observed at 2.24 ~ 2.52 and at 1.6 ~ 1.3 above the silicon nitride valence band, respectively. Also, electron traps are appeared at the 1.2 ~ 1.3 and 2.2 below the silicon nitride conduction band. Hydrogenation and nitridation processes for a control of the traps were demonstrated by plasma enhance chemical vapor deposition (PECVD). It has been achieved that memory traps could be influenced by hydrogenation and nitridation, effectively. Taking the results into considering, the energy band diagram and the identification of memory traps in SONOS structure are suggested.

D/PII.47 SILICON NANOPARTICLES IN THERMALLY ANNEALED THIN SILICON MONOXIDE FILMS

A. Szekeres(a), A. Paneva(b), T. Nikolova(a), A. Cziraki(c), Gy. Kovacs(d), I. Lisovskyy(e), D. Mazunov(e), I. Indutnyy(e), P. Shepeliavyi(e), (a)Institute of Solid State Physics, Bulgarian Academy of Sciences, Tzarigradsko Chaussee 72, Sofia 1784, Bulgaria, (b)Sofia University, Faculty of Physics, Blvd. Bouchier 5, Sofia 1126, Bulgaria, (c)Eotvos Lorand University, Solid State Physics, Pazmany P. s. 1, 1117 Budapest, Hungary, (d)Res. Institute for Techn. Phys.&Mat. Sci., Konkoly T. 29, Budapest 1121, Hungary, (e)Institute of Semiconductor Physics, National Academy of Sciences of Ukraine, Prospekt Nauki 45, Kiev 252028, Ukraine

One of the new trends in Si-based technologies is fabrication of nano-particles for non-volatile memories or light emission devised. Amorphous silicon oxides films have found a new area of application in connection with the possibility of obtaining Si nano-particles embedded in SiO matrix. Thermal annealing of SiO films is one of the simplest ways to form nanocrystalline silicon clusters. Appearance of photoluminescence (PL) bands related to Si nanocrystallites in annealed SiO films has attracted wide interest due to potential application of such material in Si-based optoelectronic devices.

Our recent work is focused on fabrication of thin SiO films with embedded Si nanoclusters. In this paper we present results on the study of thin SiO films by applying spectral ellipsometry, XRD and TEM methods. The SiO films were deposited on c-Si substrates by thermal vacuum evaporation of SiO powder. In order to form Si nano-inclusions in the oxide matrix the films were thermally annealed in Ar atmosphere at 700 and 1000oC for 5 and 30 min. It has been established that during annealing the films undergo densification and Si nano-particles are formed. The temperature of 700oC favours the coagulation of Si atoms into amorphous clusters, while 1000oC leads to their crystallization. From the X-ray scattering measurements it was concluded, that both, the as-deposited and annealed SiO films are “XRD-amorphous”, which means that the size of Si nanocrystallites is to small and/or their volume fraction is too low. This conclusion was proved by the TEM results, which show small-sized crystalline Si nanoclusters, and by the ellipsometric modelling results, which detect a volume fraction of ~2 % for Si in crystalline phase.

D/PII.48 EFFECTS OF ELECTROSTATIC COUPLING BETWEEN NANOCRYSTALS OF MEMORY STRUCTURES

A.S. Cordan, Y. Leroy and B. Leriche, PHASE-ENSPS, Pôle API, BP 10412, 67413 Illkirch, France

Quantum effects have become very important in microelectronics, both to preserve classical behaviour in MOS-like transistors and to introduce new devices. Among these new devices, nanocrystal memories or non-volatile memories were subject to great interest on fabrication research level, but less on the theoretical point of view.

Here, we want to present our model for the tunneling conduction of electrons through a nanocrystal layer placed between two electrodes which can be metallic or not. Such a model is valid for the floating gate structure in nanocrystal memories as well as for single-electron semiconducting devices. Our model is based on physical and geometrical parameters of the device under study. In this way it is quite easy to include the geometrical disorder resulting from the fabrication process of nanocrystals. Using to these parameters, we can compute quantities like energy levels in nanocrystals, tunneling rates of insulator junctions or charging effects. Then by solving the master equation associated with this device, we can obtain its electrical characteristics. To illustrate our model, we present our first calculations which show that electrostatic coupling between nanocrystals has to be taken into account for subsequent study of floating gate memory structures.

D/PII.49 NONVOLATILE MEMORY CHARACTERISTICS OF SINGLE- AND MULTI- LAYERED Si NANOCRYSTALS PREPARED BY ION BEAM SPUTTERING AND ANNEALING

Suk-Ho Choi, Yong Min Park, and Sung Kim, College of Electronics and Information and Institute of Natural Sciences, Kyung Hee University, Suwon 449-701, Korea, Kyung Joong Kim and Dae Won Moon, Nano Surface Group, Korea Research Institute of Standards and Science, P.O.Box 102, Yusong, Taejon 305-600, Korea

Ion beam sputtering has been used to fabricate single- and multi- layered SiO(2)/SiOx, which have been subsequently annealed to form Si nanocrystals (NCs) in the SiOX layer. The flat-band voltage shift, ΔV(FB) of C-V curves is found to be closely related with the PL peak energy for 50-period SiOx/SiO(2) multilayers by changing the x value determined with in-situ X-ray photoemission spectroscopy. In the single-layer devices, reduction of tunnel-oxide thickness strongly enhances ΔV(FB). An asymmetry exists between electron and hole storage, the latter being more easy. The control oxide is also a important factor for enhancing ΔV(FB), particularly in the hole charge state. The retention time is improved by increasing the thickness of the tunnel oxide rather than the control oxide. The defect states in these devices are considerably reduced by hydrogenation passivation, enhancing ΔVFB. The retention time is extended by fabricating doubly-stacked memory structures, which seems to result from suppressed charge leak between the upper NC layer and the substrate due to an energy barrier of the lower NC layer.

This work was supported by the National research program for the 0.1 Terabit Non-Volatile Memory Development sponsored by Korea Ministry of Science & Technology.

D/PII.50 PHOTOLUMINESCENCE OF SILICON NANOCRYSTALS: TIME DEPENDENT BEHAVIOUR

S. Godefroo, M. Hayne, J. Maes and V.V. Moshchalkov, Pulsed Field Group, Laboratory of Solid State Physics and Magnetism, K.U. Leuven, Celestijnenlaan 200 D, 3001 Leuven, Belgium; M. Zacharias, Max-Planck Institut für Mikrostrukturphysik, Weinberg 2, 06120 Halle, Germany

Photoluminescence (PL) is used to study the electronic properties of Si nanocrystals, formed after the thermal annealing of Si/SiO2 layers [1]. The PL spectra of different samples show a peak in the 1.4 -1.6 eV range when excited with the 351.1 and 363.8 nm lines of an argon ion laser. PL experiments as a function of time are done at temperatures between 4.2 K and room temperature and different laser power densities. An increase in the PL intensity and a shift of the center of mass as a function of time has been observed. The PL intensity can increase by a factor of up to 16 and the shift of the center of mass can amount to 228 meV on timescales of hours. The time at which saturation occurs depends on the temperature and the laser power density used.

[1] M. Zacharias et al. Appl. Phys. Lett. 80 (2002) 661.

D/PII.51 ELECTRICAL AND STRUCTURAL CONDITIONS FOR BETTER MEMORY EFFECTS OF Ge NANOCRYSTALS IN A METAL-OXIDE-SEMICONDUCTOR

S. Kim(a), S.-H. Choi(a), K.H. Cho(b), C.J. Park(b), D.Y. Kim(b), W.C. Yang(b), H.Y. Cho(b), and R.G. Elliman(c), (a)College of Electronics and Information and Institute of Natural Sciences, Kyung Hee University, Suwon 449-701, Korea, (b)Quantum-functional Semiconductor Research Center and Dept. of Physics, Dongguk University, Seoul 100-715, Korea, (c)Electronic Materials Engineering Department, Research School of Physical Sciences and Engineering, Australian National University, Canberra ACT 0200, Australia

Nonvolatile memory structures containing Ge nanocrystals (NCs) produced by ion-implantation and annealing have been characterized by capacitance-voltage, transmission electron microcopy, energy dispersive x-ray spectroscopy, secondary ion mass spectrometry, deep level transient spectroscopy (DLTS), and isothermal current

transient spectroscopy (ICTS). The memory effects strongly depend on the implant dose and the oxide thickness in metal-oxide-semiconductor (MOS) devices containing Ge NCs. For a sample implanted with a Ge dose of 1x10(16) Si.cm(-2), the capacitance-voltage curve shows a maximum flat-band voltage-shift of about 20V when the peak position of the Ge profile is very close to the SiO(2)/Si interface. The memory effects are also influenced by implantation-induced deep-level defects and SiGe complex formed at the SiO(2)/Si interface, as confirmed by DLTS and ICTS. Diffusion of Ge ions by annealing induces an accumulation of Ge NCs at the interface, having a great influence on their electrical properties in MOS devices. Possible physical mechanisms on the memory effect are discussed to explain the experimental results.

D/PII.52 POST-ANNEALING SILICON NANOCRYSTAL FORMATION ON SiOx(x<2) LAYERS DEPOSITED FROM SiH4-N2O RF DISCHARGES

M. Bedjaoui, B. Despax, LGE, Toulouse France, M. Caumont, LPS, Toulouse France and C. Bonafos, CEMES, Toulouse France

Si nanoclusters (nc) embedded in SiOx have been produced by thermal annealing of SiOx thin films prepared by PECVD at low temperature. The film composition is controlled by varying the SiH4/N2O flow rate ratio ?. Physico-chemical, structural and optical properties of SiOx, films, as deposited and annealed at 1000°C in N2 gas for 1h, were investigated by FTIR, Raman, ellipsometry and TEM. The IR spectrum for annealed sample exhibits an evolution from almost SiO2, at the lowest ?, to SiOx (x<2) at a higher ?. Raman spectra indicate that the SiOx, films exhibit the amorphous state of the as-deposited samples and a mixture of two phases, amorphous matrix and nc Si of the annealed samples. When ? decreases, the nc Si size decreases by a few nm. The optical constants (n, k) of SiOx films are obtained by fitting ellipsometry measurements with an appropriate model, Bruggeman or Forouhi model. As-deposited films consist of amorphous SiOx layers whereas annealed films can be modeled as mixtures of poly-Si crystals, a- SiOx and SiO2. It confirms the special behavior of Si nc. By increasing ?, the Si volume fraction increases and the SiO2 volume fraction decreases. TEM analyses have demonstrated that Si nc with a mean radius of 4nm are highly concentrated in annealed samples.

D/PII.53 FORMATION OF BURIED INSULATING ISLAND-LIKE SILICON OXIDE LAYER IN SILICON

A.V. Frantskevich, N.V. Frantskevich, Belarusian National Technical University, 220063 Minsk, Belarus, A.K. Fedotov, A.V. Mazanik, Belarusian State University, 220050 Minsk, Belarus, E.I. Rau and V.S. Kulinkayskas, Moscow State University, 119899 Moscow, Russia

At the present time there are three technologies (SIMOX, BESOI, Smart-Cut) of production of silicon-on-oxide structures. We propose alternative method to create buried SiO2 layer in silicon based on the gettering of oxygen from an external source onto the buried defect layer induced by preliminary hydrogen implantation.

In this work radiation defects in 20 W×cm р-type Cz Si at a depth of 0.8-1 mm were created by hydrogen ion implantation with energy of 100 keV. Then oxygen diffusion from an external source and its gettering on radiation defects were realized. The investigation of oxygen depth distribution in obtained Si/Si1-xOx+Si/Si structure was done by SIMS and RBS methods. Visualization of buried electrical active defects formed at a depth corresponding to Rp of the implanted hydrogen was performed by SEM in Surface-Electron-Beam-Induced-Voltage (SEBIV) mode. Estimation of electrical properties of SiO2 layer was carried out by the measurement of I-V characteristics.

Friday, June 3, 2005 — Morning
Vendredi 3 juin 2005 — Matin

Session XI : Novel concepts
Session chair: R. Gwilliam

D-XI.01 9:00 -Invited-

RECENT ADVANCES IN NANOPARTICLE MEMORIES

D. Tsoukalas, P. Dimitrakis, S. Kolliopoulou, P. Normand, Inst. of Microelectronics, NCSR Demokritos, 15310 Aghia Paraskevi, Greece, and School of Applied Sciences, NTUA, 15780 Zografou, Greece

Nanoparticle memories have made their point during last years as a possible solution to overcome the scaling issue of electronic nonvolatile memories. The replacement of the continuous polysilicon layer of a conventional flash memory device by a nanoparticle layer presents several advantages that will be reviewed. Ultimately, we are dealing with nanoparticle memories to significantly decrease the voltage needed to write/erase the memory without compromising its retention characteristics. Several approaches have been reported for semiconductor nanoparticle formation using techniques such as Chemical Vapor Deposition, Molecular Beam Epitaxy or sputtering. Emphasis will be placed on a silicon nanoparticle memory resulting from low-energy ion implantation of silicon into a thin oxide layer and subsequent annealing. This process allows for the formation of a two-dimensional array of silicon nanoparticles within the gate oxide practically in a single processing step making the process attractive for CMOS integration. Material issues related with ion implantation energy, dose and annealing ambient for optimum device performance will be addressed. As an alternative to semiconductor nanoparticles, metallic nanoparticles have been investigated since they have the potential for more versatile work function engineering that would allow improved data retention for memory devices operating at low voltages. Processing approaches for metallic nanoparticle formation and their integration at the device level will be addressed and corresponding memory device performance will be discussed. Finally, conclusions and further research initiatives for advancing the field will be presented.

D-XI.02 9:30

STRUCTURAL PROPERTIES OF GE-IMPLANTED SIO2 LAYERS AND RELATED MOS MEMORY EFFECTS

S. Duguay, J.J. Grob, A. Slaoui, Laboratoire PHASE, 23 rue du Loess, BP 20 CR, 67037 Strasbourg Cedex 2, France

Silicon dioxide (SiO2) layers with embedded nanocrystals (ncs) can be fabricated using several methods, including deposition, sputtering and ion implantation techniques. Due to its high compatibility with current Complementary Metal-Oxide-Semiconductor (CMOS) technology, ion implantation with subsequent annealing is a well suited method for nc-memory fabrication. In this work, SiO2 on Si layers with embedded Ge-ncs have been fabricated using Ge+-implantation and annealing. High-resolution transmission electron microscopy (HR-TEM) and Rutherford Backscattering Spectroscopy (RBS) have been used to study the Ge-redistribution in the SiO2 films as a function of annealing temperature and implantation dose. A near-Si/SiO2-interface Ge-ncs monolayer has been formed under specific annealing conditions. Independently of implantation dose, the Ge-nc monolayer is situated at approximately 4 nm from the Si/SiO2 interface. The nc density and size have been measured by TEM and RBS to be respectively few 10^12 /cm^2 and 5 nm. Capacitance-voltage and current voltage measurements on such implanted SiO2 layers metal-oxide-semiconductor (MOS) structure have been used to study their electrical properties. The results indicate a strong memory effect due to the presence of near-interface Ge-nc. Few volts flat-band shifts can be obtained at relatively low programming voltages. Long retention times have also been measured. The role of substrate doping type is discussed.

D-XI.03 9:45

EFFECTS OF OXIDIZING ANNEALING CONDITIONS ON PHOTOLUMINESCENCE OF Si NANOCRYSTALS OBTAINED BY LOW-ENERGY ION BEAM SYNTHESIS IN THIN SiO2

M. Carrada and V. Paillard, Laboratoire de Physique des Solides (LPST), Paul Sabatier University, 118 route de Narbonne, 31062 Toulouse, France; C. Bonafos and H. Coffin, nMat Group, CEMES-CNRS, 29 rue J. Marvig, 31055 Toulouse, France

Nonvolatile memory structures containing Ge nanocrystals (NCs) produced by ion-implantation and annealing have been characterized by capacitance-voltage, transmission electron microcopy, energy dispersive x-ray spectroscopy, secondary ion mass spectrometry, deep level transient spectroscopy (DLTS), and isothermal current transient spectroscopy (ICTS). The memory effects strongly depend on the implant dose and the oxide thickness in metal-oxide-semiconductor (MOS) devices containing Ge NCs. For a sample implanted with a Ge dose of 1x10(16) Si.cm(-2), the capacitance-voltage curve shows a maximum flat-band voltage-shift of about 20V when the peak position of the Ge profile is very close to the SiO(2)/Si interface. The memory effects are also influenced by implantation-induced deep-level defects and SiGe complex formed at the SiO(2)/Si interface, as confirmed by DLTS and ICTS. Diffusion of Ge ions by annealing induces an accumulation of Ge NCs at the interface, having a great influence on their electrical properties in MOS devices. Possible physical mechanisms on the memory effect are discussed to explain the experimental results.

D-XI.04 10:00

THE EFFECTS OF OXIDATION CONDITIONS ON STRUCTURAL AND ELECTRICAL PROPERTIES OF SILICON NANOPARTICLES OBTAINED BY ULTRA-LOW ENERGY ION IMPLANTATION

J. Grisolia(a), M. Shalchian(b,c), G. BenAssayag(b), H. Coffin(b), C. Bonafos(b), S. M. Atarodi(c), and A. Claverie(b), (a)LNMO-INSA, 31077 Toulouse, France, (b)CEMES-CNRS, 31055 Toulouse, France, (c)Sharif University of Technology, Tehran, Iran

Nanometer-scale electronic devices are one of the future alternatives of the conventional electronics. In these devices, the Coulomb blockade effect and other quantized charging features are exploited to improve the functionality and density of integrated circuits. However, these features must operate at room-temperature to make single-electron devices practical for applications. In this purpose, Si nanocrystals (ncs) embedded in ultra-thin SiO2 layers have recently attracted much attentions. Among several techniques, previous studies demonstrate that a combination of ultra-low energy silicon implants (1keV) and annealing at several hundred °C in diluted oxygen allows the fabrication of ultra-small ncs into a good quality thin silicon dioxide layer. In this paper, we investigate the effect of annealing conditions on the structural and electrical characteristics of a limited number of addressed silicon ncs. The structural characteristics are studied by using cross-sectional TEM and plane-view electron energy loss spectrum images of the ncs layers. The electrical measurement are performed at room-temperature by probing the I-V and I-t characteristics of nano-sized MOS capacitors containing the ncs which are formed by patterning of nano-sized contact (100nmx100nm) over the samples using e-beam nanolithography. Under these conditions, the sensitivity to discrete charging effects of a single or few ncs is observed on the I-V curves which exhibit special features including negative differential resistance (NDR) and discrete sharp current peaks. These features have been associated to discrete charging of ncs and electrostatic interaction of the trapped charges and the tunnelling current. Finally, these features are related to the annealing conditions of the ncs.

D-XI.05 10:15

FABRICATION OF 100NM GATE LENGTH MOSFET'S USING A NOVEL CARBON-NANOTUBE-BASED NANO-LITHOGRAPHY

J. Derakhshandeh(a),Y. Abdi(a), S. Mohajerzadeh(a), J. Koohsorkhi(a) and M.D. Robertson(b), (a)Thin Film Lab, University of Tehran, Tehran, Iran, (b)Department of Physics,Acadia University, Nova-Scotia, Canada

We report realization of nanometric NMOS transistors using a novel carbon-based nano-lithography technique. Vertically aligned carbon nanotubes are grown on Si substrates in a DC-PECVD apparatus using a mixture of acetylene and hydrogen at a pressure of 1-3torr and at 650oC. Nickel is used as the seed of CNT growth with a typical thickness of 2-10nm. The grown nanotubes are coated with titanium-oxide deposited with atmospheric pressure CVD, followed by silver thermal-deposition. The latter bilayer buries the nanotubes and a mechanical-polishing step is needed to re-expose them. After exposure of the buried nanotubes, they are partially removed using a plasma ashing technique. During this step part of the exposed carbon is burned in oxygen plasma and partially hollow tube is formed by the encapsulating TiO2/Ag layer. This structure is used for electron emission from sharp CNT tips placed in the center of a semi-hollow tube forming a "beam-shape" emission. This electron beam has a diameter less than 100nm and it is exploited for electron-beam writing on electro-resist substances. The purity and crystalline quality of the CNTs were investigated using TEM and SEM analyses, conforming a vertical multi-wall CNT growth. The electron-emitting tips were placed opposite to a resist-coated substrate and by applying proper voltage the trace of emitted electrons is registered on the resist. By proper mechanical manipulation we can draw lines with a width of 60nm, suitable for MOSFET gate definition. This method has been used to prepare MOSFET devices with a gate length of 100nm on 1017cm-3 P-type (100) Si substrates. Gate oxide is thermally grown SiO2 with a Cox of 1µF/cm2 and the electrical characteristics of the device show a current of 100µA/µm at 1 V drive.

10:30 **BREAK**

Session XII : Defect/impurity engineering
Session chair: L.A. Marques

D-XII.01 10:50 -Invited-

BORON DIFFUSION, CLUSTERING AND INTERACTION WITH POINT DEFECTS AND IMPURITIES IN SILICON

D. De Salvador, E. Napolitani, G. Bisognin, A. Carnera, MATIS - INFM and Dipartimento di Fisica, Università di Padova, Via Marzolo 8, 35131 Padova, Italy, E. Bruno, S. Mirabella, G. Impellizzeri, F. Priolo, MATIS - INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, Italy

The ion beam modification, widely used both for devices production (such as doping) or as analysis tool, hugely increases the point defect population in crystalline Si driving non-equilibrium processes such as Transient Enhanced Diffusion (TED) and clustering (which are limiting phenomena for the junction scaling) or causing even more intriguing phenomena such as Room Temperature (RT) dopant migration.

We'll review the most relevant recent advances in this field, and our experimental investigations aimed to describe the formation and dissolution of B clusters generated by ion implantation in c-Si. Interstitial (I) injection were promoted by Si ion implantation and annealing on MBE Si samples with B-delta-doped superlattices and with highly B doped layers. By appropriate modeling of the B diffusion profiles, the mechanisms of the point defect diffusion, their interaction with intrinsic traps and the formation and dissolution of boron clusters are quantitatively described and discussed comparing with recent theoretical calculations. Recently we have demonstrated that substitutional boron in silicon can migrate even at RT and below, stimulated by an high I flux. The B migration occurs for long distances during SIMS profiling of MBE-B deltas in c-Si at RT. Our data have a twofold implication. Through a non-conventional use of SIMS, we measure some fundamental quantities of B-RT diffusion, and provide clear evidences of B-impurities interaction at low temperature, such as trapping by C and O. At the same time strong cooling of the sample during the analysis suppresses the B-RT diffusion providing a new and very accurate profiling methodology that forces to reconsider the observations obtained in the last decades by SIMS in light of possible long-range migration artefacts.

D-XII.02 11:20

B IMPLANTED AT ROOM TEMPERATURE IN CRYSTALLINE SI: B DEFECT FORMATION AND DISSOLUTION

L. Romano, A.M. Piro, M.G. Grimaldi, MATIS - INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, Italy

D-XII.03 11:35

SUPPRESSION OF BORON INTERSTITIAL CLUSTERS IN SOI USING VACANCY ENGINEERING

A.J. Smith(a), B. Colombeau(a), R. Gwilliam(a), N.E.B. Cowern(a), B.J. Sealy(a), E. Collart(b), S. Gennaro(c), M. Bersani(c), M. Barozzi(c), (a)Advanced Technology Institute, University of Surrey, Guildford GU2 7XH, U.K., (b)Applied Materials UK Ltd, Horsham RH13 5PX, U.K., (c)ITC-irst, Via Sommarive 18, 38050, Povo (Trento), Italy

Future CMOS device requirements beyond the 65nm node entail the activation of boron in PMOS source/drain regions to concentrations well above solubility. Excess interstitials remaining after low-energy implantation in crystalline silicon drive the formation of boron-interstitial clusters (BICs) at concentrations well below solubility during the initial stages of the thermal cycle. The conventional method of overcoming this problem is to use pre-amorphization (PAI) and solid phase epitaxial SPE regrowth. However, this leads to end-of-range defect formation with concomitant source-drain deactivation during subsequent thermal steps, as well as the presence of defects in device channel regions. A potentially superior approach is the use of high-energy co-implantation (for example with Si ions) to suppress BIC formation by generating an excess of vacancies in the boron-implanted region. Recent work has shown that it is possible to optimise vacancy generation using lower energy co-implants than previously reported.

In this paper we report on the effects of medium-energy Si co-implants on an ultra-low energy (500eV) boron implant in a SOI substrate. The results are characterised using differential Hall measurements, SIMS and RBS analysis to determine the degree of activation, atomic concentration profiles and substrate damage, respectively. A wide temperature study shows very large improvements in electrical activation at low temperatures (600°C). The effects of excess vacancies decrease with higher temperatures due to the increase in solubility and diffusion. The Rs/Xj values approach those obtained by PAI with none of the problems associated with PAI.

D-XII.04 11:50

EFFECT OF FLUORINE ON BORON THERMAL DIFFUSION IN THE PRESENCE OF POINT DEFECTS

M.N. Kham, H.A.W. El Mubarek, P. Ashburn, School of Electronics & Computer Science, University of Southampton, Southampton SO17 1BJ, U.K. and J.M. Bonar, Innos Ltd, Mountbatten Building, Highfield, Southampton SO17 1BJ, U.K.

With an increased interest in the use of fluorine co-implantation with boron for MOSFET devices, it is important to understand the mechanisms by which fluorine reduces boron diffusion. Mechanisms such as B-F chemical reaction, vacancy-fluorine clusters and fluorine-interstitials interactions have been proposed in the literature. In this paper, a point defect injection is done to investigate the mechanism responsible for boron thermal diffusion suppression in F+ and B+ implanted silicon. A 5keV, 7x1012 cm-2 B+ implant into silicon is used which is typical for halo implants in n-MOS. Three F+ energies, 5, 50 and 185keV are used. It is followed by rapid thermal annealing at 900 ~1000oC for different times in N2 for an inert anneal and O2 for injection of interstitial point defects from the surface. Fluorine profiles for samples implanted with 185keV F+ and annealed in N2 show two fluorine peaks at ~Rp and ~Rp/2. Under interstitial injection, the Rp/2 peak decreases in size and for long anneal times is completely eliminated, supporting an earlier claim that the Rp/2 peak is due to vacancy-fluorine clusters. For fluorine implant energies at 5 and 50keV, no fluorine remains after annealing for 60s at 1000oC. Suppression of boron thermal diffusion is observed for 5 and 50keV F+ implants but for the 185 F+ energy, the boron profile shows anomalous enhanced diffusion at concentrations lower than 1x1017 cm-3.

D-XII.05 12:05

STUDY OF FLUORINE SEGREGATION AND INCORPORATION DURING SOLID PHASE EPITAXY OF Si

G. Impellizzeri, S. Mirabella, E. Bruno, F. Priolo, MATIS-INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, 95123 Catania, Italy, E. Napolitani, A. Carnera, INFM and Dipartimento di Fisica, Università di Padova, Via Marzolo 8, 35131 Padova, Italy

In Si-based microelectronic technology, the exceptional shrinkage demanded for future devices fabrication also requires a reduction of junction depths. To this purpose, different approaches are investigated. Among these, the F capability in reducing the B transient enhanced diffusion (TED) in silicon is widely recognized, even if the microscopical mechanism by which this phenomenon occurs has not been unambiguously explained.

We report a study on the F incorporation in Si during solid phase epitaxy (SPE) at 580 °C, in presence of B and/or As, clarifying the F incorporation mechanism in Si. In undoped samples, a strong segregation of F at the moving of the amorphous-crystalline interface has been characterized, leading to a SPE rate retardation and to a consistent F loss through the surface. In B or As doped samples, an enhanced, local F incorporation is observed in the doped region, while it misses in the case of B and As co-implantation (that leads to a compensating dopant effect). We demonstrated that the above enhanced F incorporation is due to a kinetic effect related to the SPE rate modification by doping, while the hypotheses of a F–B or F–As chemical bonding are refused. These results shed new light on the application of F in the fabrication of ultra-shallow junctions in future generation devices.

12:20 **CLOSING**

12:30 **LUNCH**