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E-MRS Spring Meeting 2004
May 24-28, 2004

SYMPOSIUM C

New materials in future silicon technology

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E-MRS 2004 SPRING MEETING

SYMPOSIUM C

Tuesday, May 25, 2004 Morning

Session I: Materials challenges I
Session chairs: J. Fompeyrine

09:00 **WELCOME**

C-I.1 09:10 -INVITED- DEVICES ARCHITECTURES AND MATERIALS FOR NANOCMOS AT THE END OF THE ROADMAP AND BEYOND

S. Deleonibus, CEA-LETI DTS, CEA-Grenoble, 17 rue des Martyrs, 38054 Grenoble, Cedex 09, France

The strong association of new materials and devices architectures is the condition of success of significant breakthroughs in future nanoelectronics. Since 1994, the International Technology Roadmap for Semiconductor (ITRS) [1] has been accelerating the scaling of CMOS devices to lower dimensions despite the difficulties that appear in device optimization at the sub 20nm level [2, 3]. Breakthroughs are required to continue scaling at the same rate. Which are the main showstoppers for CMOS scaling? Short channel effects and tunneling in the gate dielectric are at the origin of the showstoppers. Channel, gate stack and source and drain engineering have to be reconsidered for new devices architecture issues. FD SOI and Strained channels [4] are among the envisaged solutions to enhance the Ion/Ioff trade of. Metal gates show promising perspectives [5] to avoid gate dopant depletion. The issue of electron mobility degradation in the channel of HiK isolated MOSFETs is still a problem to be solved [5]. Supply voltages lower than 1V will require FDSOI architectures (single or multi gate) and threshold voltage adjust by tuning the gate material workfunction. Laser or Flash Annealing, Plasma Doping will be required to minimize parasitic effects. It will be very difficult to compete with CMOS logic because of the low series resistance required [6]. Due to the important charge retention capabilities, trapping phenomena in Silicon Nanocrystals are exploited for Flash memory applications [7]. By introducing new materials, Si based CMOS will scale beyond the ITRS [1] as the future System-on-Chip Platform integrating new disruptive devices. Single Electronics will be a major research subject.

[1] ITRS 2001Edition.
[2] S. Deleonibus et al., EDL pp. 173, April 2000.
[3] G. Bertrand et al. ULIS 2003 Udine.
[4] T. Ernst et al. Symp VLSI Tech., pp 51-52, June 2003, Kyoto (Japan).
[5] B. Guillaumot et al., IEDM 2002, pp. 355-358, Dec 2002, San Francisco (USA).
[6] M. Sanquer et al. SNW 2003, pp. 70-71 Kyoto (Japan).
[7] B. de Salvo et al., IEEE TED, vol. 48, pp. 1789, 2001.

C-I.2 09:50 CAN WE MOVE UV ABSORPTION EDGE OF SILICA GLASS TO SHORTER WAVELENGTHS?

A.J. Ikushima and K. Saito, Toyota Technological Institute, Tempaku-ku, Nagoya-city, Japan

Microlithography by using laser light has been extended to as shorter wavelengths as possible for achieving as higher memory density as possible. The next step of the laser-microlithography should be done by using F2 excimer laser, which emits light at 157 nm. As far as glass is concerned, silica glass should be the exclusively sole candidate material that may be used at this wavelength, although nature appears rather mean to us in the sense that UV absorption edge of silica glass is just around that wavelength.

We have revealed that any properties of silica glass including UV absorption edge are strongly influenced by the fictive temperature, which is the temperature where silica glass is frozen to the glass state. We prepared silica glass samples with various fictive temperatures, and measured the UV absorption as a function of wavelength changing temperature. The UV absorption edge at a certain temperature shifts to a shorter wavelength with decreasing the fictive temperature. That is, as the degree of disorder in silica glass structure decreases, silica glass gets more transparent at 157 nm, say. Moreover, doping of F or Cl very efficiently lowers the fictive temperature, making silica glass more transparent at that wavelength. We will propose silica glass that can be used fomicrolithography of next generation at 157 nm.

10:10 **BREAK**

C-I.3 10:20 -INVITED- POST HAFNIUM OXIDE TECHNOLOGY FOR HIGH-K GATE DIELECTRICS

Hiroshi Iwai, Frontier Collaborative Research Center, Tokyo Institute of Technology, 4259, Nagatsuta-cho, Midori-ku, Yokohama 226-8502, Japan

Significant increase in the gate leakage current of MOSFETs are becoming the most critical issue which limits the downscaling of CMOS LSI, and the replacement of SiO_2 gate insulator with that of High-k is the urgent item to be realized as the solution. Although there are still so many problems to be solved for the high-k dielectrics to be used in commercial products, so far, hafnium silicates with nitrogen involvement are regarded as the most promising high-k materials and expected to be introduced within several years. However, even with the hafnium silicates, it is not easy to realize equivalent oxide thickness below 1 nm, which has to be applied in several years. Thus, the research also for the post hafnium oxide dielectrics are becoming important. Fortunately, lanthanum oxides have been found to be the most probable candidate both

from the theoretical and experimental preliminary results. In this paper, MOS capacitor and transistor characteristics with lanthanum oxide gate insulator as the post hafnium oxide is described.

10:50 **COFFEE BREAK**

Session II: High-K dielectrics theory
Session chairs: R. Elliott

C-II.1 11:20 -INVITED- TOWARDS THE DESIGN OF HIGH-K DIELECTRICS FROM *AB INITIO* CALCULATIONS

Wanda Andreoni, IBM Zuerich, Switzerland

The need of extending the downscaling of CMOS field-effect transistors to physical thicknesses of 1–2 nm has recently spurred tremendous activity in the search for an alternative to silicon dioxide as gate dielectric and in the investigation of the fundamental materials-science issues. This talk will cover very recent studies carried out with *ab initio* calculations of electronic, structural and vibrational properties of several high-*k* oxides, such as silicon oxynitrides and aluminates with diverse compositions. In particular, these results provide not only a detailed understanding of the factors that determine the dielectric constant of these materials but also suggestions for novel high-*k* materials to be fabricated.

12:00 **LUNCH BREAK**

Tuesday, May 25, 2004 Afternoon

Session III: High-k dielectrics I
Session chairs: D. Schmeißer

C-III.1 14:00

DIELECTRIC PROPERTIES OF NANOMETER-THICK INSULATING LAYERS: A REFLECTION ELECTRON ENERGY LOSS SPECTROSCOPY APPROACH

M. Gautier-Soyer(a), F. Paumier(a), M.J. Guittet(a), G. Tan(b), R.H. French(b,c), Y.M. Chiang(d), A. Ramos(d), M. Tang(d), S.Y. Chung(d), L. DeNoyer(e), (a)Service de Physique et de Chimie des Surfaces et des Interfaces, DSM-DRECAM-SPCSI, CEA Saclay, 91191 Gif sur Yvette Cedex, France, (b)Dept of Materials Science and Engineering, University of Pennsylvania, Philadelphia PA, USA, (c)Experimental Station, DuPont Corporation Central Research, Wilmington DE, USA, (d)Deconvolution and Entropy Consulting, Ithaca NY, USA, (e)Dept of Mat. Sci. and Engineering, Massachussets Institute of Technology, Cambridge MA, USA

Due to the increased miniaturization of silicon-based devices, increasingly thinner dielectrics are used, and it is a challenge to characterize properly insulating films of nanometer thickness. In this respect, Reflection Electron Energy Loss Spectroscopy (REELS) can be very powerful, as the probing depth is of the same order as the thickness of the film. Indeed, besides a direct measurement of the band gap in the depth of one nanometer, an estimate of the optical dielectric constant characteristic of the ultra-thin film can be obtained as well. We present a REELS study of the dielectric properties of ultra-thin oxide layers formed onto a Si single crystal, where the oxidation has been performed under well-controlled thermodynamic conditions allowing getting an equilibrium surficial film.

This work was partially founded by EU Commission Contract G5RD-CT-2001-00586, in cooperation with NSF Award DMR-0010062.

C-III.2 14:20

EFFECTS OF NITRIDATION OF THE HIGH-K OXIDES IN MOSFETS: DENSITY FUNCTIONAL STUDIES

Jacob Gavartin(a), Adam Foster(b) and Alexander Shluger(a), (a)Department of Physics and Astronomy, University College London, Gower street, London WC1E 6BT, U.K., (b)Laboratory of Physics, Helsinki University of Technology, Finland

Introduction of high dielectric oxides as gate materials would allow for further miniaturization of field effect transistors. However, performance of high-k MOSFET prototypes suffers from the flat band potential instability associated with charged defects in the oxide. Post deposition annealing (PDA) of the oxide films in nitrogen contained ambient is considered to be the way of reducing this effect. However, there is little understanding of the role of nitrogen in relevant oxides, and the experimental data on nitridation are often conflicting.

In this paper we present density functional molecular dynamics simulations of nitrogen contained defects in the monoclinic HfO2 and discuss their influence on electric properties of the oxide. Assuming various nitrogen sources, we study the interaction of atomic and molecular nitrogen, ammonia and nitric oxide molecules with the host lattice. We further consider migration and various dissociation reactions with and without presence of anion vacancies and interstitial defects. Calculations suggest that nitrogen anneal of the oxides may lead to an effective immobilisation of native defects. However, nitrogen in molecular form is unlikely to significantly reduce the residual charge in the bulk film. In contrast, an atomic nitrogen, having larger solubility, may lead to a formation of oxynitride films with larger thermal and chemical stability.

C-III.3 14:40

STOICHIOMETRY AND FERMI LEVEL PINNING AT Si:HIGH K OXIDE INTERFACES

J. Robertson, P. W. Peacock, Engineering Dept, Cambridge University, Cambridge CB2 1PZ, U.K.

High dielectric constant or 'high K' oxides are needed to replace silicon dioxide as the gate oxide in future CMOS devices [1]. There is intense effort to implement high K oxides in CMOS technology in the 65 nm node by 2005. Many challenges remain. The favoured oxide is HfO2 or Hf silicate. The interface between the high K oxide and the Si channel is seldom abrupt, it contains a few monolayers of SiO2. Highly doped poly-Si is presently used as the gate electrode. The interface of the poly-Si and the high K oxide is abrupt. It has recently been found that the Fermi level is pinned at this back interface [2]. It is speculated that this may be due to gap states due to Si-metal bonds at the interface. This has led to the belief that high K oxide cannot be implemented with poly-gates and that metal gates are required, a critical industrial decision [3]. We have previously calculated the electronic structure of a wide range of ideal O- or Hf-terminated Si:HfO2 interfaces [4,5]. Configurations giving no states in the gap are identified. This allows us to define the perfect and non-perfect interface structure. We have now calculated the electronic structure of some interfaces with defects and configurations that give states in the gap.

1. G Wilk, R M Wallace, J M Anthony, J App Phys 89 5243 (2001) 2. C Hobbs et al, Tech digest VLSI symp(2002) 3. P Chou, Intel press announcement 4. P W Peacock, J Robertson, Phys Rev Letts (2004) 5. P W Peacock, J Robertson, App Phys Lett 83 5497 (2003)

C-III.4 15:00

INTERFACE STATES ENERGY DISTRIBUTION IN (100)SI/HFO2

Y.G. Fedorenko, L. Truong, V.V. Afanas'ev, A. Stesmans, Department of Physics, University of Leuven, Belgium

We applied quasistatic (QS) capacitance-voltage (CV) analysis to estimate interface states distribution (Dit) on energy (E) in MOS structure with the semiconductor surface switched to the inversion by corona charging. It has been found that the classical Berglund method can be used to reliably assess Dit over the energy range from ~0.2 to 0.9 eV above the silicon valence band using just MOS capacitors of one type of Si conductivity in combination with supply of the minority charge carriers from the periphery of the capacitor. This procedure has been tested on the Si/SiO2 and Si/HfO2 interfaces demonstrating that the density of states can be reliably obtained. Being applied to the (100)Si/HfO2 interfaces the method reveals a significant impact of the CVD fabrication process on the density of interface states including both the Si dangling bond defects

(Pb0 centers) and the insulator-related traps. The measurement frequency range can be extended to the low-kHz range, if capacitors of smaller area are used, thus making the technique highly promising for quick Dit evaluation at the interfaces of Si with high-k insulators.

C-III.5 15:20

LONG-TIME STABILITY OF THIN Pr(x)O(y)-FILMS ON Si(100) GROWN BY PULSED LASER DEPOSITION

D. Wolfframm, M. Ratzke, M. Kappa and J. Reif, LS Experimentalphysik II, BTU Cottbus, and JointLab IHP/BTU, Universitaetsplatz 3-4, 03044 Cottbus, Germany

For further downsizing the physical equivalent gate-oxide thickness for CMOS transistors many difficulties are expected. One of the biggest concerns is the increase of direct-tunnelling leakage current as the gate dielectric layer becomes thinner. Also, the long-time stability of thin dielectric films is most important for application and can be crucial for electrical performance. We have studied the long-time stability of thin PrxOy-films on Si(100), produced by Pulsed Laser Deposition from sintered Pr6O11 targets. In particular, the surface morphology, the chemical layer/interface composition, and the electrical properties were investigated. For PrxOy films grown at 650 °C substrate temperature, we find clear evidence of a change in surface morphology with time after film preparation: while the surface immediately after deposition is characterized by large splashes (mainly Pr2O3) superimposed on a background of mixed oxides (Pr2O3, Pr6O11), later on, the surface becomes more homogeneous. No similar effect was observed for layers grown at 900 °C substrate temperature indicating a more stable, none-reactive surface (Pr2O3). An analysis of XPS spectra (Pr 3d, O 1s, Si 2p) showed that not only the line shape of the Pr 3d and O 1s core level spectra changed but also the Pr 3d/O 1s intensity ratio. This transition of chemical environment suggests the formation of Praseodymium Hydroxide. Since Pr6O11 is well known for its strong hygroscopic behaviour, Pr(OH)3 will preferably be formed between the splashes (Pr2O3), accompanied by the appearance of PrO2.

C-III.6 15:40

PROPERTIES OF ZrSixOy THIN FILMS PREPARED BY LASER ABLATION

M. Filipescu(a), N. Scarisoreanu(a), D.G. Matei(a), G. Dinescu(a), A. Ferrari(b), M. Balucani(b), M. Dinescu(a), (a)National Institute for Laser, Plasma and Radiation Physics, PO Box MG–16 Magurele, Bucharest 77125, Romania, (b)INFM, Unit E6, University "La Sapienza", Rome, Italy

Thin films of zirconium silicate were obtained by alternative ablation of Zr and Si targets in oxygen reactive atmosphere; in a set of experiments a radiofrequency (RF) discharge beam was added to the Pulsed Laser Deposition system. Pt coated silicon was used as collector. The influence of deposition parameters as laser wavelength (355 nm and 532 nm), laser fluence (4-6 J/cm^2) and oxygen pressure (10^{-3}-10^{-2} mbar) on the deposited layers properties was studied. The RF beam addition influence on the electrical, optical and morphological proprieties of zirconium silicate films was particularly investigated. The obtained films, with thicknesses in the range of 15-60 nm, have been characterized by Secondary Ions Mass Spectroscopy (SIMS), Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), X-ray diffraction (XRD) and electrical measurements. Dielectric permittivity values (real part) in the range of 7-13 and low losses were evidenced for samples prepared with the radiofrequency oxygen beam addition. The leakage current was also found to strongly depend on the deposition parameters.

16:00 **COFFEE BREAK**

Session IV: High-k dielectrics II
Session chairs: H. Iwai

C-IV.1 16:30

CHARACTERIZATION OF INTERFACE STATES IN AMORPHOUS La2Hf2O7 GATE DIELECTRIC

G. Vellianitis(a), A. Dimoulas(a), G. Apostolopoulos(a), G. Mavrou(a), J.C. Hooker(b), Z.M. Rittersma(b), (a)MBE Lab, Institute of Materials Science, NCSR “DEMOKRITOS”, Athens, Greece, (b)Philips Research Leuven, Belgium

In this work, we investigate the electrical behavior of the amorphous high-k gate dielectric La2Hf2O7, which is deposited on rapid thermal SiO2 (RTO) / Si(001) as well as on bare Si(001) substrates using an RF plasma source of atomic oxygen in an MBE chamber. The C-V and G-V curves measured in MIS capacitors were analyzed using a recently developed multi-frequency model [1], where the Poisson and Schrödinger equations are solved self consistently taking into account the effect of electrically active interface states. From the fitting procedure, we can extract values for the EOT, VFB, the carrier capture cross-section cn,p and the energy distribution of interface traps in the gap. The main advantage of the model is that it can be used in MIS structures with high density of defects and high leakage current, where conventional methodologies based on quasi-static C-V measurements are inadequate.

Low EOT values were obtained for samples grown on bare Si substrates. In as-grown films, the measured EOT was found to be as low as 0.7nm at Tg = 600C, with gate current Jg = 2x10-1 A/cm2 @ 1V accumulation. Analyzing the complex admittance measurements for samples deposited on RTO/Si substrates, we estimated that the capture cross section of holes at interface traps was about 4x10-16 cm2, a value which is typically obtained for the SiO2/Si interface. Interestingly, for the samples deposited directly on Si, the estimated capture cross-section values differ substantially indicating that the nature of defects is different. Finally, it was found that the interface states density Dit increases with dielectric thickness. Similar behaviour is observed after forming gas annealing, although lower Dit values were obtained. [1] G. Apostolopoulos et.al., Appl. Phys. Lett., 84, 260 (2004)

C-IV.2 16:50

INLUENCE OF THE ORDER-DISORDER TRANSITION IN Y2O3/SI THIN FILM ON THE INTERFACIAL REACTIONS

F. Paumier, R.J. Gaboriaud, F.P. Pailloux, Laboratoire de Métallurgie Physique, Université de Poitiers, CNRS-SP2MI, BP 30179, 86962 Chasseneuil-Futroscope cedex, France

Y2O3 has attracted much attention because of several physical properties (high k value (10-18), wide band gap (5.5 eV)) particularly relevant for MOS structure. Y2O3 thin films are deposited by ion beam sputtering on Si. This deposition technique promotes a very particular structure in the thin films whatever the substrate. It has been shown that two cubic crystallographic phases coexisted (fluorite fm3m and cubic C Th7). The fm3m cubic phase is due to a strong disorder of the oxygen network induced by the argon bombardment during the growth (penning effect). After annealing under air or vacuum only the cubic C structure is observed. This work pays a particular attention to the interfacial reactions between Y2O3, SiO2 and Si. It has been shown that the phase transformation in the Y2O3 thin film induces a particular behavior of the Y2O3/SiO2/Si interfacial reactions with a reduction of the SiO2 when the film is annealed under vacuum. Nevertheless a silicate inter-layer is observed at the interface when the sample is annealed in air. A comparative study is made between interface observations and the order disorder transition in the Y2O3 film by means of HRTEM observations and EELS spectrometry. These observations are compared with the evolution of the dielectric constant and the electric oxide charges in the structure.

C-IV.3 17:10

PR4F OCCUPANCY AND VB/CB BAND OFFSETS OF PR$_{2}$O$_{3}$ AT THE INTERFACE TO SI(001) AND SIC(0001) SURFACES

Dieter Schmeißer, Angewandte Physik - Sensorik, BTU Cottbus, Postfach 10 13 44, 03044 Cottbus, Germany, H.-J. Müssig, IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Resonant photoelectron spectroscopy (PES) at the Pr4d and Pr3d absorption edges is used to study the electronic properties at the interface of epitaxial grown Pr$_{2}$O$_{3}$ on Si(001). We compare these results to Pr$_{2}$O$_{3}$ films grown on SiC(0001) surfaces.

In the electronic structure of bulk Pr$_{2}$O$_{3}$ the valence band (VB) states are predominantly of Pr6s and O2p atomic parentage. Weak contributions from Pr4f states are identified from the strong increase the VB features at the Pr4d and Pr3d resonances. They are the consequence of mixed valency caused by ligand-to-Pr4f charge transfer states. On SiC(0001) surfaces Pr$_{2}$O$_{3}$ films are prepared by a wet chemical treatment. Here the oxide forms an amorphous layer. There is an intermediate range of about 1nm thickness in which a silicate is formed. At the Si(001) interface in-situ prepared epitaxial layers (d$\leq$5nm) enable us to study the contribution of the Pr4f electronic states in the valence band population as a function of layer thickness. We also find a silicate intermediate. We conclude that the silicate causes an enhanced hybridization (covalent bonding) of the Pr4f states into the valence band. In our coverage dependent data the offset in the VB maxima is determined from the relative position of the valence band spectra. We find an offset of 2eV as well as a 1eV increase in the electron affinity caused by an interface dipole moment. The offset of the conduction bands is deduced from the onset of the Si2p and Pr4d XAS data, it is of the order of 2eV again. Our data allow to derive a full description of the interface properties of that high K material, a prerequisite for its possible application in storage, logic, and power electronics.

C-IV.4 17:30

SOLID STATE REACTION BETWEEN PR AND SIO2 STUDIED BY PHOTOELECTRON SPECTROSCOPY AND AB INITIO CALCULATIONS

D. Schmeißer, Angewandte Physik-Sensorik, BTU Cottbus, PF 10 13 44, 03013 Cottbus, Germany and G. Lupina, J. Dabrowski, H.-J. Müssig, IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Gate dielectrics containing a Pr silicate may possibly replace SiO2 in sub-0.1 mm CMOS technology. The oxidation of Si(001) during Pr2O3 deposition produces a stable silicate buffer layer with the substrate interface resembling the SiO2/Si(001) interface, but the process is difficult to control. Here we show that it is possible to convert an industrial quality, ultrathin SiO2 into a silicate by Pr deposition.

The reaction between SiO_2 and Pr has been investigated by a non-destructive depth profiling using synchrotron radiation and XPS, and by ab initio calculations. About 1 nm of Pr was deposited on top of about 2 nm thick SiO_2/Si(001) films. The reaction is initiated at the outer SiO_2 surface, as expected from ab initio analysis. At room temperature, a Pr silicide and a Pr oxide are formed and SiO_2 is partially reduced. Annealing at moderate temperatures leads to the formation of a silicate which is stable up to ~ 800oC. The silicide, which should be avoided in interface design, is completely transformed to silicate at elevated temperatures. Ab initio results confirm the thermodynamical stability of a Pr silicate with respect to decomposition into Pr_2O_3 and SiO_2.

C-IV.5 17:50

PHYSICAL AND ELECTRICAL CHARACTERIZATION OF POLYSILICON VS. TiN GATE ELECTRODES FOR HfO_2 TRANSISTORS

Patrick S. Lysaght, Jeff J. Peterson, Brendan Foran, Chadwin Young, Gennadi Bersuker and Howard R. Huff, International SEMATECH, Materials Evaluation Test Structures, 2706 Montopolis Drive, Austin TX 78741-6499, USA

The effects of pre-deposition substrate treatments and gate electrode materials on the properties and performance of high-k gate dielectric transistors were investigated. The O_3 vs. HF-last/NH_3 pre-deposition treatments and polysilicon vs. TiN gate electrode performance were systematically studied in devices consisting of HfO_2 gate dielectric produced by atomic layer deposition. High-Angle Annular Dark Field Scanning Transmission Electron Microscopy (HAADF-STEM) using X-ray spectra and Electron Energy Loss Spectra (EELS) were used to produce elemental profiles of N, O, Si, Ti, and Hf to provide interfacial chemistry information and convey changes in concentration across these high-k transistor gate-stacks of 1.0 to 1.8 nm equivalent oxide thickness (EOT). EELS spectra illustrate an apparent overlap of elements; however, this phenomenon is not greater than the interfacial roughness dimension for the TiN electrode case while an amorphous reaction region was produced at the HfO_2/polysilicon interface likely at the expense of the HfO_2 layer quality. We also present fast transient electrical measurements designed to characterize the electron trapping behavior of these samples. The data clearly indicate significantly more trapping (corresponding to more trap centers) associated with the polysilicon electrode. This is the case regardless of the substrate pre-treatment and may be related to an increased physical thickness of the dielectric film, as illustrated by HAADF STEM-EELS and consistent with the approximately 0.5 nm higher EOT associated with polysilicon electrodes on otherwise identical gate stacks. In addition, charge trapping is greater with polysilicon electrode devices due to higher density of trap centers induced by high-k/polysilicon materials interactions.

C-IV.6 18:10

APPLICATION OF Ru-BASED GATE MATERIALS FOR CMOS TECHNOLOGY

M. Tapajna, P. Pisecný, R. Luptak, K. Husekova, K. Frohlich, L. Harmatha, J. C. Hooker, F. Roozeboom, Institute of Electrical Engineering, SAS, Dubravska cesta 9, 841 04 Bratislava, Slovak Republic, Faculty of Electrical Engineering and Information Technology, STU, Ilkovicova 3, 812 19 Bratislava, Slovak Republic, Philips Research Leuven, Kapeldreef 75, 3001 Leuven, Belgium, Philips Research Eindhoven, WA 1, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands

Together with high-k dielectric films, metal gate electrodes have to be employed in advanced CMOS technologies. The metal gate material should be carefully selected with respect to work function, stability of metal-dielectric stack and compatibility with the CMOS process. In our investigation, Ru, RuO_2 and $SrRuO_3$ gate electrodes grown on thermal SiO_2, atomic-layer deposition (ALD) Al_2O_3 and HfO_2 dielectric films have been analyzed by means of high-frequency and quasi-static capacitance-voltage (C-V) measurement as well as by current-voltage (I-V) characteristics of MOS capacitors. The Ru-based gate materials were prepared by metal-organic chemical vapor deposition (MOCVD) at temperatures between 250 and 500°C.

Work function of the investigated gate material, leakage current, density of effective defect charge as well as density of interface traps of the gate oxide film were extracted from the measurements. These properties are discussed with regard to application of the Ru-based metal gates in CMOS technologies.

Wednesday, May 26, 2004 Afternoon

Session V: Non-volatile memories I
Session chairs: A.J. Ikushima

C-V.1 14:00 -INVITED-

NON-VOLATILE MEMORY TECHNOLOGIES: EMERGING CONCEPTS AND NEW MATERIALS

R. Bez, STMicroelectronics, Non-Volatile Memory Technology Development, Central R&D, Via C.Olivetti 2, 20041 Agrate Brianza (Milan), Italy

The non-volatile memory technology is becoming more and more important in the semiconductor industry, due to the application in electronic portable equipments (like mobile phones, palm top, notebook, mp3 audio player, digital camera and so on) and it will be one of the main drivers of the technology scaling.
The current mainstream is based on the Flash technology that it is expected to be the reference technology also for the next few years. Nevertheless Flash has some technological and physical constraints that make more difficult their further scaling.
In this contest is growing the industrial interest for new technologies, that exploit new materials and physical storage concepts that go beyond the pure CMOS technology and the electron charge transport, as it happens today in Flash.
Hence in the first part of the presentation the main emerging non-volatile memory technologies based on inorganic material, like Ferroelectric Memory (FeRAM), Magnetoresistive Memory (MRAM) or Phase Change Memory (PCM) and the main innovative concepts based on organic material like ferroelectric or conductance switching polymer will be analyzed.
Instead the second part will be focused on the Phase Change Memory technology, as one of the best candidate due to the large spectrum of application, covering the main characteristics, like bit size, writing time, reliability, scalability, and presenting the latest development results.

C-V.2 14:40 -INVITED-

CURRENT EFFECTS IN MAGNETIC LAYER STRUCTURES

R. Elliott, Theoretical Physics, University of Oxford, 1 Keble Road, Oxford OX1 3NP, U.K.

Magnetic layers coupled through a non magnetic spacer show interesting and important properties, including giant magneto resistance, depending on the relative orientation of the magnets. This depends on the coupling transmitted by the spacer and it is known that such coupling can be significantly affected if a current is driven through the junction. In certain circumstances the coupling changes sign as the current is increased and can therefore be used to switch orientations. Such structures are therefore potential candidates for MRAM cells. The theory of these effects and their possible application to MRAM for both conducting and non-conducting (magnetic tunnel junction) spacers will be reviewed.

15:20 **BREAK**

Session VI: Non-volatile memories II
Session chairs: L. Risch

C-VI.1 15:30 -INVITED-

CHARGE TRAPPING MEMORIES FOR FUTURE HIGH DENSITY NON-VOLATILE MEMORY APPLICATIONS

M. Specht, Infineon Technologies AG, Corporate Research, Otto-Hahn-Ring 6, 81730 Munich, Germany

High density data storage for mobile applications increasingly drives the aggressive scaling of non-volatile semiconductor memories. The dominating technology is still based on floating gate cells that are currently fabricated with smallest feature sizes of F = 130 nm allowing for densities up to 1Gbit/chip in NAND architecture. Shrinking this cell type to the 90 and 70 nm technology node is expected, however, it faces serious design challenges mainly due to the tunnel oxide thickness which can hardly be reduced. To achieve even higher memory densities various alternative memory approaches (MRAM, resistive memories, etc.) are currently investigated. In this talk, we focus on charge trapping memory devices that currently experiences great interest. Inherently, these devices permit reduced voltages due to the smaller total dielectric thickness compared to floating gate devices and, in addition, they offer the possibility of multi-bit storage. We present and discuss new materials and alternative device concepts based on charge trapping that give new perspectives for very high density non-volatile memories beyond the 70 nm technology node.

C-VI.2 16:10

EXPERIMENTAL EVIDENCE OF SI NANOCLUSTER DELTA-LAYER FORMATION IN BURIED AND THIN SIO2 FILMS BY ION IRRADIATION

Lars Röntzsch, Karl-Heinz Heinig, and Bernd Schmidt, Research Center Rossendorf, Dresden, Germany

Since Tiwari's pioneering work on multidot flash memories [1], huge effort has been put into the synthesis of Si nanoclusters (NCs) in the gate oxide of a MOSFET substituting the common poly-Si floating gate. Si NCs act as individual charge traps, thus, improving the device chracteristics. To assure a sharp threshold voltage during charging, all NCs must be equally placed at a distance of ~3nm from the transitor channel. Previously, we presented a theoretical concept suggesting that a suitable Si multi-dot structure can be achieved in a two-step process compatible with CMOS technology [2,3]. Irradiating Si ions of medium energy through a layer stack of 50nm poly-Si, 15nm SiO2, and the Si substrate leads to collisional mixing in the oxide. During annealing, the Si-SiO2 interfaces recover rapidly. Excess Si remaining in the oxide grows up to a Si-NC delta-layer (DL). Due to the low mass contrast of tiny Si NCs to SiO2, the Si-NC-DL structure is outside the visibility limit of common XTEM.
Here, we present evidence (including XTEM) which proves the mechanism of Si-NC-DL formation. For reasons of mass contrast enhancement a 5nm Ge layer was inserted in between the capping and the oxide layer. During ion irradiation, Ge atoms are mixed into the oxide. During annealing, the Ge monomers diffuse through the oxide and attach to Si NCs due to the favorable Si-Ge bond. Differently from DLs of pure Si NCs, the SixGe(1-x)-NC-DL is indeed observable in XTEM due to the higher mass contrast to SiO2. Without

tiny Si NCs to which Ge attaches, no NC DL would be found. Thus, the existence of Si NCs which align in a collective manner at a distance of ~3nm from the Si channel is proven. [1]Tiwari,APL68,1377(1996) [2]Heinig,APA,77,17(2003) [3]Schmidt,Heinig: EU Patent 1070768A1

C-VI.3 16:30 PARTIAL SELF-ORDERING MECHANISM IN Si QUANTUM DOTS FORMED BY CHEMICAL VAPOUR DEPOSITION: IMPACT ON THE THRESHOLD VOLTAGE DISTRIBUTION OF NANOCRYSTAL MEMORIES

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We have studied the formation of Si quantum dots by chemical vapor deposition of silane on SiO2 in the regime of the sub-monolayer depositions and of surface coverages of about 20 - 30%. Several substrate temperatures, post-deposition annealing temperatures, and substrate preparation conditions have been studied. Energy filtered transmission electron microscopy (EF-TEM) with very high spatial and chemical resolution is adopted to evaluate the dot size and inter-dot distance distributions. It is shown that the nucleation process, though continuous under typical deposition conditions, is not a random process. Indeed, the inter-dot distance distribution shows a clear maximum at finite distance values, i.e., the dots are separated by Si-free denuded zones. We show that the dot size scales with the size of its own capture zone. The effect is most likely related to the silicon adatoms diffusivity, and it will be shown and discussed in the framework of a scaling model, based on a modification of the classical Voronoi tessellation approach [1]. In nanocrystal memory devices, it has been proposed that the dispersion from cell to cell of the surface fraction (Fdot) covered with Si dots in the gate area is the main limitation for nanocrystal memory scaling [2]. This dispersion affects the threshold voltage (VT) distribution in the nanocrystal memory array. In the presence of a non-random dot nucleation, with Si-free capture zones around each dot, the dispersion of the Fdot distribution is, in fact, lower compared to the case of random nucleation. This difference is quantified, compared to data, and extrapolated to small gate area values.

16:50 **COFFEE BREAK**

17:00 **POSTER SESSION I**

C/P01-C/P13: Gate dielectrics and gate materials

C/P01 DEFECT CHARACTERIZATION OF ULTRATHIN OXIDE LAYER ON SILICON WAFERS BY LOW-PHOTOPERTURBED SCANNING CAPACITANCE SPECTROSCOPY

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The fabrication of advanced complimentary-metal-oxide-semiconductor (CMOS) devices needs the formation of ultrathin gate oxide layer with good uniformity and breakdown strength. One of the factors leading to breakdown problem of gate oxide layer is the interface defects induced by metallic contamination. In this work, we have provided low-photoperturbed scanning capacitance spectroscopy (LPSCS) extended from scanning capacitance microscopy (SCM) to investigate the interface defects for ultrathin SiO2 on Si wafers contaminated by iron. Subsequent to the standard RCA cleaning procedure, slight iron contamination was introduced on the wafer surface of studied samples. Right after the contamination and dry processes, an ultrathin thermal oxide layer, 4 nm in thickness, was grown on the wafers. By reducing the photoperturbation of SCM, one can significantly enhance the influence of interface defects on spectroscopic signals. For n- and p-type wafers, the LPSCS profiles revealed that the dominant interface defects induced by iron contamination are donor-type interface traps. Experimental results indicated that the LPSCS with nanometeric resolution is a reliable method to characterize ultrathin SiO2 on Si wafers. It is also revealed that the influence of these interfacial traps on the electrical characteristics of the MOS capacitor cannot be observed by conventional capacitance-voltage measurement. The evidently experimental results will be shown and discussed.

C/P02 PROPERTIES OF HIGH-K DIELECTRIC MATERIALS STUDIED BY CONDUCTING ATOMIC-FORCE MICROSCOPY

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The steadily shrinking device dimensions in semiconductor industries demand for advanced electrical characterization methods operating on the nanometer scale. One suitable technique already used for the evaluation of silicon gate oxide quality [1] is Conducting Atomic-Force Microscopy (C-AFM).

Here, C AFM is used to study different high-k dielectric materials with regard to their electric properties and homogeneity. Therefore, materials like ZrO2 and HfO2, grown by atomic layer chemical vapor deposition on a silicon substrate are studied by C-AFM in ultra high vacuum (UHV). The UHV conditions are mandatory to avoid surface modifications during the experiments. Local current-voltage measurements are used to obtain a statistical distribution of the leakage current as a function of voltage. This provides an insight into the influence of the amorphous or crystalline structure of the films depending on their thickness and heat treatment. Further, two dimensional current scans with a positive voltage applied to the sample are performed to obtain the local distribution of leakage current. [1] S. Kremmer, C. Teichert, E. Pischler, H. Gold, F. Kuchar, M. Schatzmayr, Surf. and Interf. Anal. 33 (2002), 168.

C/P03 LOW-TEMPERATURE AND HIGH-QUALITY RADICAL ASSISTED OXIDATION TECHNOLOGY FOR HIGH PERFORMANCE STRAINED SiGe/Si MOSFETS

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A low-temperature (< 700 °C) and high-quality radical-assisted oxidation (RAO) process for the growth of ultrathin (1.4 - 3.7 nm) gate-oxides was successfully developed utilizing a remote ultraviolet ozone source. The MOSFETs with RAO gate oxides showed improved device characteristics (e.g. 27 - 67 % enhanced Gm) and oxide reliability (22 - 53 % reduced Vth shift and 30 – 38 % reduced Gm degradation after electrical stress), in comparison with the devices with non-RAO or standard furnace oxides. In particular, the transistor with a RAO gate oxide maintained superior device properties even after oxide’s soft

breakdown. The 1/f noise characterization result confirmed that the RAO gate oxide was less defective before and after soft breakdown. Finally, the RAO process was applied to the fabrication of strained Si0.8Ge0.2 p-channel MOSFETs requiring a low thermal budget oxidation process. It was shown that the process could suppress the Ge segregation when the Si-cap layer was thinned to 2 nm, which greatly improved the device's performance. The RAO process has a great potential in producing a high-quality and high-reliability ultrathin base oxide in two-layer gate dielectric stacks for strained SiGe/Si MOSFETs.

C/P04 ELECTRON STATES AT THE (100)Ge/HfO_2 INTERFACE

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The significant progress recently made in the development of high-permittivity non-native insulators for silicon metal-oxide-semiconductor (MOS) devices may open new bright possibilities if these materials could be successfully transferred to other semiconductors for which MOS applications previously failed because of lacking a good native gate insulator. Among these Ge attracts most of the interest because its inherent high bulk carrier mobility may be used to compensate for any channel mobility degradation routinely encountered in Si MOS devices with gate insulators different from SiO2. Here we report on the analysis of the electronic structure of the interface of (100)Ge with deposited HfO2, the feasibility of which is considered for MOS applications. Both the band- and defect-related electron states were characterized through determining their energy distributions using complementary experimental methods: the internal electron photoemission spectroscopy (IPE) and the ac conductance/capacitance-voltage (GV/CV) measurements. The IPE suggests that the 0.66-eV wide Ge bandgap is located close to the middle of the 5.6-eV wide HfO2 bandgap with the offsets of the conduction and valence bands inferred as 2.0 and 3.0 eV, respectively. The valence band offset is reduced by ~1 eV after post-deposition annealing, but remains sufficiently high to block the hole injection. At the same time, the CV/GV analysis shows that this anneal is highly beneficial in reducing the density of Ge/HfO2 interface traps distributed in the Ge bandgap.

C/P05 INTERFACE STATES DENSITIES AND ELECTRICAL LOSSES IN La-Hf BASED HIGH-K DIELECTRICS ON SILICON

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This paper investigates the interface trap density of a new high-k gate dielectric stack, La2Hf2O7/SiO2 on silicon. Amorphous La2Hf2O7 thin films are deposited by metal evaporation in the presence of an atomic oxygen beam on an ultra-thin 1.5 nm SiO2 layer grown by rapid thermal oxidation on a p-type Si substrate. Complex characterisation comprising measurements of capacitance and conductance versus voltage at different frequencies were performed and interface states densities (Dit) were inferred using the conductance method. For the samples with the thinnest gate oxide and having the gate voltage as a parameter, the G/ vs. frequency characteristics revealed a peak structure involving a double peak. The peak behaviour varies with the gate bias. One peak is related to interface states losses whereas the second peak, which is atypical in silicon dioxide-based MOS capacitors, can be related to a quantum mechanical tunnelling phenomenon.

C/P06 DEPOSITION OF THIN TITANIUM DIOXIDE FILMS AND ITS KINETICS STUDY

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We report a kinetics study of the deposition of thin titanium dioxide films on Si (100) by a technique of ultraviolet-assisted injection liquid source chemical vapor deposition using ultraviolet with 222 nm radiation. The alkoxide precursor titanium isopropoxide (TTIP) was dissolved in cyclehexane, and then driven into the reaction chamber by an argon carrier gas, while nitrous oxide was used as an oxidizing agent. The properties of the films deposited have been studied using ellipsometry, Fourier transform infrared spectroscopy, X-ray photoelectron spectroscopy and UV spectrophotometry. The effect of substrate temperature, reaction time, the flow rate of N2O and the concentration of precursor was studied.

C/P07 INFLUENCE OF THE DEPOSITION CONDITIONS ON THE PROPERTIES OF TITANIUM OXIDE PRODUCED BY RF MAGNETRON SPUTTERING

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The search for new dielectric materials to be used metal-insulator-semiconductor (MIS) structures to replace the silicon oxide (SiO2) has been growing up. The aim is to use materials with high dielectric constants that could allow the use of thicker films to reduce the role of leakage currents in devices using very thin SiO2 layers.

In this work we present data concerning the production of titanium oxide (TiO2) thin films by rf sputtering that present suitable characteristics to be used in gate dielectrics, alone or in a mixed tandem structure, taking advantage of its high dielectric constant. The influence of the deposition conditions (argon/oxygen gas flows, deposition pressure and rf power) on the films properties, namely band gap, interface states, permissivity, resistivity were studied. Films with low flat band voltage (less then 2V) were obtained, indicating good interface properties. An optical band gap of 3.3 eV was obtained which is a value close to the band gap of stoichiometric titanium oxide (around 3.2 eV). Compactness was studied by spectroscopic ellipsometry (SE) and the results related with the deposition conditions. Results concerning the application of this material in a mixed structure with aluminium oxide (Al2O3) for gate dielectric applications will be also shown.

C/P08 FIRST INVESTIGATIONS OF MIM CAPACITORS USING Pr_2O_3 DIELECTRICS

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Metal-insulator-metal (MIM) capacitors with Pr2O3 as high-k material have been investigated for the first time. We varied the thickness of the Pr2O3 layers as well as the bottom electrode material. The layers are characterized using x-ray photoelectron spectroscopy, x-ray diffraction, transmission electron spectroscopy and secondary ion mass spectroscopy.

The electrical characterization shows that Pr2O3 MIM capacitors can provide higher capacitance densities than Si3N4 MIM capacitors while still maintaining comparable voltage coefficients of capacitance. The Pr2O3 dielectric material seems to be suitable for use in silicon RF applications.

C/P09

A COMBINED SYNCHROTRON X-RAY DIFFRACTION AND STM STUDY OF THE STRUCTURAL PROPERTIES OF ULTRA-THIN PRASEODYMIUM OXIDE LAYERS ON Si(111)

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Epitaxial praseodymium oxide layers on Si(001) are currently studied as potential high-k dielectrics to replace silicon dioxide in future microelectronics devices. To better understand this system, the higher evolved long-range order of praseodymium oxide layers on Si(111) allows their use as model systems in comparative studies. Here, a thickness-dependant grazing incidence X-ray diffraction study of the heteroepitaxial system praseodymium oxide/Si(111) over the technologically important thickness range (1-10 nm) is presented. Specular theta-2theta scans show that these oxide layers are determined by the growth of the hexagonal praseodymium oxide phase (space group:P-3m1) which is attached with its (001) plane to the Si(111) substrate surface. However, strong evidence is given by these scans that also the cubic praseodymium oxide phase (space group: Ia3) is present growing with its (111) plane on the Si(111) substrate. Measurements of in-plane reflections have been applied to study the azimuthal orientation of these oxide phases and to determine the evolution of the lattice parameters over the studied thickness range. These studies are supplemented by STM and LEED experiments focussing on submonolayer deposits.

C/P10

GROWTH OF LANTHANUM OXIDE FILMS FOR APPLICATION AS A GATE DIELECTRICS IN CMOS TECHNOLOGY

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We have investigated properties of insulating lanthanum oxide (La2O3) films in connection with the replacement of silicon oxide (SiO2) gate dielectrics in new generation of CMOS devices. The La2O3 layers were grown using metalorganic chemical vapour deposition (MOCVD) at temperatures 400 – 600 °C. X-ray diffraction analysis revealed polycrystalline character of the films grown above 500 °C. Surface morphology was studied by atomic force microscopy. High-frequency and quasi-static capacitance-voltage and current-voltage characteristics were used to analyse electrical properties of as-grown and post-annealed La2O3 layers. Density of effective defect charge, interface trap density, leakage currents and dielectric constant were extracted from the measurements. Electrical properties, in particular dielectric constant of the MOCVD grown La2O3 is discussed with regard to the film preparation conditions.

C/P11

EFFECT OF MAGNETIC METAL CLUSTER DOPING ON DIELECTRIC PROPERTY ENHANCEMENT OF $LaAlO_3$ THIN FILMS PREPARED BY PULSED LASER DEPOSITION

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The thin films of Ni-doped dielectric LaAlO3 by a co-ablation of magnetic metal Ni and dielectric LaAlO3 (LAO) on silicon-based substrates have been prepared by pulsed laser deposition. A significant enhancement of the dielectric constant of LAO upon a Ni-doping is found. Furthermore, the dielectric modulation by applying a magnetic field to the samples is observed, obviously due to the ferromagnetism of Ni metal clusters embedded in the LAO thin films. A series of microstructural and dielectric characterizations on the as-prepared thin films have been performed and the mechanism underlying the dielectric enhancement upon the Ni-doping is discussed.

C/P12

DEVELOPMENT OF SOL-GEL MgO THIN FILMS FOR INSULATION ON SiC

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Silicon Carbide (SiC) is a wide bandgap semiconductor suitable for high-power and high-temperature devices. However, the commercialization of advanced SiC power devices remains limited due to performance limitation of the SiO2 dielectric among other issues. Indeed, SiO2 has a permittivity 2.5 times lower than that of SiC, which means that at critical field for breakdown in SiC, the electric field in the adjoining SiO2 becomes too high for reliable operation. Therefore, alternative dielectrics having a permittivity higher than or of the same order as that of SiC (k=10) should be used to reduce the electrical field in the insulator.

Among alternative dielectrics, magnesium oxide (MgO) seems to be a good candidate regarding its bulk properties : large bandgap (Eg=7.8 eV), high thermal conductivity and stability, and a suitable dielectric constant (k=10). In order to evaluate such promising candidate, the sol-gel process appears to be a convenient route to elaborate this kind of coatings. By selecting appropriate precursor solutions and controlling the temperature of heat treatment of the layers, MgO films could be obtained under various cristallisation states: amorphous-like, non-oriented and preferential [111] orientation (polycristalline). MIM structures have been used to investigate the insulating potentialities of these sol-gel MgO films. The dielectric strength of the films was found to be microstructure-dependent, and reached 5 to 8 MV/cm at room temperature. Leakage currents were measured from 100°C up to 250°C. Two conduction regimes have been identified: an-ohmic-like regime for electrical fields less than 0.3MV/cm, and a schottky-type mechanism for electrical fields between 0.3MV/cm and 1MV/cm, with zero-field potential barrier heights of the order of 1 eV.

C/P13

PREPARATION OF SrRuO3 FILMS FOR ADVANCED CMOS METAL GATES

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We report on the growth and properties of SrRuO3 films for application as metal gates for CMOS devices. The films were grown at 500 °C by metal-organic chemical vapour deposition on thermal SiO2 and atomic-layer deposited Al2O3 and HfO2 dielectric films. The films exhibit room temperature resistivity below 1 mohmcm. We have analyzed the interface between the SrRuO3 metal gate and the oxide film by Rutherford backscattering and secondary ion mass spectroscopy. Annealing in an oxygen atmosphere and forming gas (90% N2 + 10% H2) were employed for testing the stability of the SrRuO3 metal gate.

Finally, electrical chracteristics of the metal gate stack were investigated by high-frequency capacitance-voltage measurements. The properties of metal-organic chemical vapour grown SrRuO3 gate electrode are analyzed with regards to integration in CMOS devices.

C/P14-C/P24: Other front-end processes and materials

C/P14 OBSERVATION OF DISLOCATIONS IN STRAIN-RELAXED SILICON-GERMANIUM THIN FILMS WITH FLAT SURFACES GROWN ON ION-IMPLANTED SILICON SUBSTRATES

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Strained Si grown on a relaxed SiGe layer is an attractive material because of its potential for high carrier mobility. Dislocations must be introduced to relax the SiGe. However, it is also important that no dislocations exist around the SiGe surface; otherwise the dislocations would grow into the strained Si layer and affect its performance. The ion-implantation technique is useful for achieving these requirements because the profile and concentration of lattice defects can be controlled accurately. Hence we implanted Ar ion into the Si substrate before the epitaxial growth of Si0.8Ge0.2 with the thickness of 100 nm by the solid source molecular beam epitaxy method. We then annealed specimens. We investigated the microstructure of SiGe/Si by transmission electron microscopy, and investigated the strain relaxation by Raman spectroscopy and X-ray diffractometry. The surface roughness was studied by atomic force microscopy. We have succeeded in fabricating almost fully relaxed Si<0.8>Ge<0.2> layers of only 100 nm thickness. The surface roughness was atomically flat with the rms roughness of 0.5 nm in the scan area of 10 μm × 10 μm. The conditions were as follows. The Ar ion-implantation energy and ion dose were 25 keV and 1 x 10<15> / cm<2>, respectively. SiGe was grown at 773 K followed by the annealing at 1173 K. It was revealed that dislocations, which were necessary for stress relaxation, formed into loops and were localized around the interface of the SiGe and Si substrate.

C/P15 INFLUENCE OF ULTRASOUND ON MECHANICAL STRESSES RELAXATION IN Si_xGe_{1-x}/Si SYSTEM AT He^+ IONS IMPLANTATION

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The ion implantation of Si+, Ge+, He+, and C+ are used to decrease the mechanical stresses in heteroepitaxial structure SixGe1-x/Si. The in-situ introduction of ultrasound (US) wave into crystal at implantation can modify physical processes of defect creation and character of their further changes at annealing significantly.

The SixGe1-x (x»0.2, d»100nm) films grown on Si substrates by CVD method at temperature 580°C have been investigated. Ion implantation of He+ with energy 50KeV at T=20°C with doses in interval 1015-1016cm-2 was performed. At implantation the US waves (6 MHz) were introduce into SixGe1-x/Si structure. The annealing in Ar (650-850°C, 60c) was fulfilled. The crystal perfection and deformation value were investigated by optical and X-ray diffraction methods. The next results were obtained: (i) ion implantation of He+ causes the stress into film which growth with dose; (ii) additional US waves influence decreases the mechanical stress growth; (iii) annealing of samples at 650-750°C stimulates the relaxation of these stresses. As main mechanisms of US waves influence (i) the stimulated diffusion of He atoms and interstitial Si atoms and (ii) creation and further transformation of defect complexes and implanted.

C/P16 FREE-CARRIER CONCENTRATION CONTROLLED BY NANOCLUSTERS IN PROTON-IMPLANTED SILICON

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Electrical properties of bistable shallow donors in monocrystalline silicon which are introduced by proton implantation followed by annealing at 300-450oC have been studied by Hall effect and conductivity measurements methods. The temperature dependences of equilibrium and nonequilibrium carrier concentration, relaxation kinetics and carrier mobility were measured. For the first time an unusual linear dependence of equilibrium concentration of free carriers in the range from 50 to 360oC is observed. The obtained experimental data demonstrate that carrier concentration in the samples is controlled by defect nanoclusters. Processes of defects diffusion and formation of nanoclusters at 450oC reduce the supersaturation with hydrogen and radiation defects and decreases free energy of crystal. These processes are inhibited in the range from 20 up to 200oC but increasing temperature in this interval causes the intrinsic energy of nanoclusters to increase linear with the temperature and induces a transition from deep level state of the nanocluster to shallow electron level state with the low thermal capacity configuration. As a result, free carrier concentration increases linearly with temperature from 1.5E15 cm-3 to ~1E17 cm-3.

C/P17 THE STRUCTURES PREPARED BY IMPLANTATION OF SILICON WITH NITROGEN AND ANNEALING UNDER HIGH HYDROSTATIC PRESSURE

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The effect of treatment at up to 1400 K under hydrostatic argon pressure up to 1.2 GPa on the structure of silicon implanted with nitrogen, Si:N (nitrogen doses, D, up to 2x10(18)cm(-2), energies up to 150 keV) was investigated by TEM, X-Ray, photoluminescence (PL) and other methods.

The high temperature-pressure treatment produces typically strongly disturbed buried nitrogen-containing layers. The treatment of Fz-Si:N samples (D=1x10(17)cm(-2), E=140 keV) at 720 K - HP results in the increased intensity of PL at 0.78 eV while the intensity of PL at 1.02 eV, 1.04 eV and 1.09 eV remained unchanged. The treatment of Fz-Si:N (D=2x10(16)cm(-2)) under HP at 1070 - 1400 K results in the presence of numerous dislocations; the intensity of dislocation-related PL at 0.81 eV increases with HP but decreases with increased temperature of the treatment. Our investigations contribute in understanding the mechanisms related to creation of insulating layers in nitrogen-implanted silicon.

C/P18 PHOTOLUMINESCENCE STUDIES OF THE DEFECTS CREATED IN NITROGEN-DOPED SILICON DURING ANNEALING UNDER ENHANCED PRESSURE

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The presence of nitrogen affects the properties of annealed oxygen-containing Czochralski grown silicon. Nitrogen admixture influences the oxygen precipitation process at enhanced temperature (HT), resulting in the changed microstructure of Cz-Si:N. This is the reason for utmost interest in Cz-Si:N in view of its application in microelectronics. Enhanced hydrostatic pressure (HP) during annealing of Cz-Si:N can result in changed nitrogen and oxygen diffusivities, solubility, out-diffusion of point defects and impurities as well as influences an interaction between the defects and impurities.
Nitrogen doping was performed during Cz-Si growth from nitrogen atmosphere or by N2+ implantation. Implantation was done at 140 keV with N2+ doses up to 1*10^18 cm-2. Cz-Si:N subjected to annealing under enhanced hydrostatic pressure (HP-HT treatment) was studied by low-temperature photoluminescence (PL) and related methods. The HP-HT treatment results the changed defect structure of Cz-Si:N (mainly in respect of creation of dislocations). The PL results were explained accounting for the amount of precipitated oxygen determined from the IR absorption measurements. Retarded out-diffusion of nitrogen and the HP-HT dependent microstructure of Cz-Si:N within an implanted region were stated. The qualitative explanation of the obtained results has been proposed.

C/P19 STUDY OF THE EFFECT OF RAPID THERMAL ANNEALING ON THE INTERACTION BETWEEN A Cr THIN FILM AND Si MONOCRYSTALLINE

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Transition metal silicides were widely used in microelectronics technology as Schottky barriers, gate electrodes, interconnects and contacts. We studied in this work, interfacial reaction between a thin layer of Cr and Si(100) substrates. The Cr film was deposited by electron gun evaporation. The samples were submitted to rapid thermal annealings in high vacuum, at different temperatures during various times from 15 s to 60 seconds.
The physico - chemical characterization of the samples was carried out by Rutherford backs catering spectroscopy and X – ray diffraction. It was showed that, the CrSi2 disilicide forms and grows until the total transformation of the Cr layer. The growth of this compound with the duration of the annealing time is linear, which lets to say that the kinetic of growth is governed by the chemical reaction. The mechanism of silicide formation is discussed.

C/P20 THE EFFECT OF SILICON ION IMPLANTATION ON THE STRUCTURE OF TANTALUM-SILICON CONTACTS

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The effect of ion beam mixing on the formation of tantalum–silicon contacts was studied. Silicon implantation into 50 nm Ta layers on n+-Si (100) was carried out at temperatures from 150 to 500°C and fluences between 1x1015 and 1x1017 Si/cm². The microstructural changes were characterized by Auger electron spectroscopy (AES), X-ray diffraction and cross-sectional transmission electron microscopy (TEM). The contact resistance was measured before and after implantation using the four-point Kelvin method. Implantation at low temperature (~150°C) leads to the formation of an amorphous Ta(Si) interface-layer. The width of the mixed layer increases linearly with implanted dose and temperature. Substrate amorphisation results in an increase of the contact resistance. An improved contact resistance was achieved by implantation with 5x1016 Si/cm² at 400°C. TaSi2 formation at the interface was observed in this case.

C/P21 EFFECT OF Sb+ IMPLANTATION ON COPPER SILICIDES FORMATION AND MORPHOLOGY AFTER ANNEALING OF Cu/Si STRUCTURES

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In this work, the solid state reaction between a thin film of copper and silicon has been studied using Rutherford backscattering spectroscopy, X-ray diffraction, scanning electron microscopy and microprobe analysis. Cu films of 400, and 900 Å thicknesses are thermally evaporated on Si(111) substrates part of them had previously been implanted with antimony ions of 5x10-14 or 5x10-15 at/cm2 doses. The samples are heat treated in vacuum at temperatures in the range 200 – 700°C for various times. The results show the growth and formation of Cu3Si and Cu4Si silicides under cristallites shape dispatched on the sample surface, independently of the implantation dose. On the other hand, it is established that the copper layer is less and less consumed as the antimony dose increases, resulting in the accumulation of Sb+ ions at silicide/Si interface and in the silicide layer close to surface. The exposure of samples to air at room temperature shows the stability of Cu4Si phase whereas the Cu3Si silicide disappears to the benefit of the silicon dioxide formation. The observed phenomena are discussed.

C/P22 HIGH STRAINED SiGe LAYER GROWN ON ULTRA-THIN SILICON-ON-INSULATOR SUBSTRATE

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An ultra-thin silicon-on-insulator (SOI) structure is a versatile substrate because a large variety of materials with small lattice and thermal expansion mismatch can be fabricated on it. In this work, a high-quality strained Si0.82Ge0.18 layer was grown on an ultra-thin SOI substrate using ultra-high vacuum chemical vapor deposition (UHVCVD). The SiGe layer is about 110nm thick exceeding the conventional critical thickness on bulk Si. Cross-sectional transmission electron microscopy (XTEM) results show that the SiGe layer is dislocation-free and the atoms at the SiGe/Si interface are well aligned. Auger depth profiling reveals that the Ge concentration remains almost constant throughout the SiGe epilayer. X-ray diffraction (XRD) results and subsequent calculations based on the experimental data indicate that the SiGe layer is highly strained and the SiGe unit cell grows in the expected tetragonal configuration to match the Si lattice.

C/P23 BORON SURFACTANT-ENHANCED GROWTH OF Si FILMS ON CaF_2/Si

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Semiconductor-insulator heterostructures are attractive for silicon-based devices such as resonant-tunneling diodes. Among these systems, CaF_2/Si heterostructures on Si substrates with a few nanometer thick films are highly promising due to the large conduction band discontinuity and the small lattice mismatch. The realization of such devices requires the growth of both ultra-thin, atomically flat CaF_2 layers on Si and Si layers on CaF_2. Growth of CaF_2 on Si (111) has been extensively studied, and atomically flat CaF_2 films have been achieved [Thin Solid Films, 410, 72 (2002)]. The epitaxial growth of Si on CaF_2 however, has been less investigated and is more difficult to achieve because the smaller surface free energy of CaF_2 makes wetting of the CaF_2 surface with Si energetically very unfavorable. In our earlier work, we have shown that by surfactant-enhanced solid-phase epitaxy (SPE) with the surfactant Sb continuous, smooth and crystalline Si films on CaF_2/Si(111) of previously unattained quality can be obtained [Appl. Surf. Sci. 211, 203 (2003)]. In this work, we have investigated the surfactant-enhanced SPE of Si thin films on CaF_2/Si(111) with the surfactant boron. We found that with this technique even better epitaxial Si layers can be achieved. By utilization of this new method for the growth of ultra-thin Si quantum-well layers in CaF_2/Si/CaF_2/ structures on Si(111), we have fabricated double-barrier resonant-tunneling diodes exhibiting negative differential resistance characteristics with a much higher peak current density than any previously reported CaF_2/Si/CaF_2 resonant-tunneling structure.

C/P24 ENHANCED MAGNETORESISTANCE RATIO and IMPROVED THERMAL STABILITY of SPECULAR SPIN VALVE with CAPPING LAYERS

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Demand for higher MR (Magnetoresistace) ratio and superior thermal stability from magnetic read head and MRAM (Magnetic Random Access Memory) increases rapidly with areal magnetic recording density. The using specualr effect is indispensable to achieve 100 Gbit/in2 areal density. The most previous researches have been focused on the precise formation of NOL (Nano Oxide Layer) in pinned layer of specular spin valve with oxidation time, oxidation pressure, and technique for oxidation. In this study, we tried to achieve better magnetic and thermal properties of specular spin valve with varying capping layers (Al and Ta).

Si/Ta5/NiFe3.5/MnIr6/CoFe2/NOL/CoFe2/Cu2.5/CoFe(t)/Cu1/Ta, Al 1-2 nm bottom specular spin valves were deposited on Si (100) substrate by auto process magnetron sputtering. The base pressure was less than 3×10-8 Torr. A NOL was formed in the load lock chamber by exposing it to pure oxygen gas. Samples were annealed for 30 min. at 578 K under 3 kOe in-plane magnetic field in a vacuum furnace, followed by cooling to room for 2 hour. In the case of Ta 2 nm capping layer, the MR ratio was saturated with 11.2 % above 3 nm free layer thickness. By reducing Ta capping layer thickness from 2 to 1 nm, the MR ratio increased from 11.2 to 12 %. This incensement of MR ratio may be due to decreasing shunt effect. On the other hand, in the case of Al 1 nm capping layer showed lower MR ratio than Ta capping layer. The highest MR ratio was obtained by using Ta 1 nm capping layer. Also we compared thermal properties of Ta and Al capping by thermal aging test. The results indicated that Ta capping is more stable than Al capping. More detailed magnetic and thermal properties of specular spin valve with capping layers will be present at the conference site.

C/P25-C/P30: Back-end processes and materials

C/P25 ATOMIC LAYER CHEMICAL VAPOUR DEPOSITION OF COPPER

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Copper films with (111) texture are of considerable importance to VLSI metallization, because copper offers lower RC delays and improved electromigration resistance. Conformal coverage of high-aspect-ratio features is also a requirement. We have, therefore, investigated the atomic layer deposition (ALD) of copper using the metalorganic complex [2,2,6,6-tetramethyl-3,5-heptandionato]Cu(II) as the source of copper and hydrogen as the reactant gas. The dependence of the microstructure of the films on ALD conditions, such as the number of ALD cycles and the deposition temperature, was studied by x-ray diffraction, scanning electron microscopy (SEM), and transmission electron microscopy. Analysis of (111)-textured films shows the presence of twin planes in the copper grains throughout the films. SEM shows a labyrinthine structure of highly connected, large grains developing as film thickness increases. This leads to low resistivity.

C/P26 EVOLUTION UNDER ANNEALING OF STRUCTURAL PROPERTIES OF W-SI-N SPUTTERED DIFFUSION BARRIERS

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Ternary W-Si-N thin layers (~ 200 nm thick) to be applied as diffusion barriers for Cu interconnections are synthesized by RF magnetron sputtering, starting from a W5Si3 target and inserting the N2 gas flow in the Ar plasma atmosphere.

The evolution of structural and functional properties under annealing is studied, in order to investigate the effects of heating on the stability of the layers. Heat treatments are performed in vacuum in the range 600 – 1000 °C. The stoichiometric composition is measured by the means of Rutherford Backscattering (RBS). Film density is obtained by combining RBS results with the measured films thickness. The higher is N concentration, the denser film is growing. Fourier Transform Infrared (FT-IR) and Raman spectroscopy are performed before and after annealing in order to study the evolution of chemical bonds. Surface morphology is investigated via Atomic Force Microscopy (AFM) and Scanning Electron Microscopy (SEM). Preliminary results on annealed layers highlighted a N depletion for samples at high N content and the blistering of the films for temperatures above 600 °C. This process seems to be strictly related both to the annealing temperature and to N concentration. The microcrystalline structure is investigated by the means of Transmission Electron Microscopy (TEM) and X-Ray Diffraction (XRD). Dynamic electrical measurements are also performed, by monitoring film conductivity in situ during annealing, in order to investigate changes in the electrical behaviour, related to the structural modifications of the layers.

C/P27 VIBRATIONAL SPECTROSCOPY CHARACTERISATION OF LOW-DIELECTRIC CONSTANT Si-O-C:H FILMS PREPARED BY PECVD TECHNIQUE

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Low dielectric a-SiOC:H films of 380 nm have been deposited from tri-methyl-silane and oxygen mixture using PECVD technique over Si substrate at 120°C temp. and pressure of 100 Torr. The deposited samples have been thermally treated in atmospheric pressure of N2 at 400°C for 30 minutes and, then, have been treated in N2 plasma at 700W rf power at the same temp. in order to form a nitride capping layer. Finally, these samples have been annealed in vacuum at some temperatures between 400°C and 900°C for 30 minutes. The structural investigation of the films was carried out by vibrational spectroscopy, i.e. Raman Spectroscopy and FT-IR Spectroscopy. FT-IR spectrum for as deposited sample reveals the presence of Si-H stretching, the combination of Si-C stretching and SiC-CH3 rocking mode, Si-O-Si asymmetric stretching, Si-CH3, C-Hx, and –OH related vibrational bands at 855 cm-1, 800 cm-1, 1034 cm-1, 1270 cm-1, 2965 cm-1, and in the range between 3250 cm-1 and 3700 cm-1, respectively. On annealing the samples up to 600°C, it is observed that the peaks around 800 cm-1 and around 1270 cm-1 are invariable with annealing temp by means of peak position and intensity, indicating the good thermal stability of this material, important during the processing for device. The Si-O-Si stretching frequency is shifting toward higher frequency on annealing the sample. The intensity of –OH related bonds (H-OH and Si-OH) is reducing with temp up to 600°C, indicating the reduction of ionic bonds which means the further decrement in dielectric constant. The Raman spectra don't show any C-C bonding at lower temp., while, annealing the sample at temp. after 500°C enables the formation of C-C bond after release of hydrogen from the sample, confirming the crystallisation of film.

C/P28

MATERIAL MICROSTRUCTURAL INFLUENCE ON SPIRAL THIN FILM INDUCTORS

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With the trend of higher operation frequencies in wireless communication (>1GHz), the integration of all discrete passive devices on a silicon substrate is a must, of which the fabrication of thin-film inductors is a challenge. Although the research on the thin-film inductor has been conducted for more than 10 years, litter research was focused on the dependence of the material microstructures on the inductor characteristics. In this paper, we fabricate planar spiral thin-film inductor by typical integrated circuit processes, and the inductor structure is fixed for the design of the optimum property. We then examine the inductor properties, including inductance and quality factor as function of the variety of the material used in the inductor and buffer layers. The materials are characterized by four-point probe, x-ray diffraction and dielectric measurement. The materials used for the inductor include copper with strongly (111) and (002) preferred orientations and different conductivities, which is compared to magnetic cobalt materials, while those for the buffer layer include silicon dioxide (SiO2), organic silicon glass (OSG) and polyimide. The results show that the ohmic loss can be effectively reduced by the better conductivity and stronger textures, which results in better quality factor at high frequencies. We also show the inductor properties also depend on the buffer layer materials. The mechanisms will be discussed in this paper.

C/P29

CHALCOGENIDE THIN FILMS FOR DIRECT RESISTORS FABRICATION AND TRIMMING

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The fabrication of thin film resistors based on Ge-Sb-Te chalcogenide alloys is proposed. By exploiting the phase change properties of the deposited film, a laser beam is used for inducing a transition from high to low resistivity along selected paths. Conductivity changes as high as four orders of magnitude can be routinely achieved. This candidates the technique for maskless fabrication of compact precision resistors on a variety of planar and non-planar substrates.

C/P30 CHEMICAL AND ELECTRICAL CHARACTERIZATIONS OF DEPOSITS ELABORATED BY FIB ASSISTED CVD

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Scaling down in microelectronics leads to the complexity increase in devices. The failure analysis step requires a tool able to modify the interconnection network of a chip to validate the circuit design.

Gaseous molecules can be locally dissociated on a surface irradiated with a tightly focused ion beam. This so-called FIB assisted CVD process is a maskless direct writing technique which allows to deposit metallic, semi-conducting or insulating patterns. Using cross beam system (coupling of converging FIB and SEM columns), it is possible to reduce the surface exposure to ion beam and to decrease damage. It is now commonly ran in industry for circuit reconfiguration. However, due to section shrinking, low resistivities are now required. We will present the chemical and in-situ electrical characterizations of 300 nm wide tungsten wires obtained from W(CO)6 precursor decomposition. These wires have a metallic behaviour, a low resistivity (15 times higher than the bulk one) and a good stability to atmosphere exposure. From the point of view of insulators, we have deposited oxide silicon films from dissociation of TMCTS (tetramethylcyclotetrasiloxane) precursor. We will present our first results in electrical and chemical analysis carried out on submicro metallic bridges (two crossing wires insulated from each other) entirely drawn by FIB assisted CVD.

C/P31-C/P32: Plastic substrates

C/P31 STUDY ON CRYSTALLIZATION OF AMORPHOUS SILICON USING CEO2 SEED LAYER PATTERNED ON THE PLASTIC SUBSTRATE

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Many researchers are working these days on crystallization of amorphous silicon (a-Si) for application of Thin Film Transistor Liquid Crystal Display (TFT-LCD) on the plastic substrate. We present our work on crystallization of amorphous silicon film using XeCl excimer laser annealing on the polyethersulfone (PES) substrate in this paper. And we are reporting CeO2 seed layer patterned such as dot and line between Si film and the PES substrate to obtain better crystallinity. Previous researches in this field have shown that laser of high energy density is required to crystallize a-Si films without using seed layer. But, we have successfully obtained the crystallization condition using laser of low energy density using a seed layer of CeO2. This paper reports this achievement in details. Also, we have drawn a comparison of a-Si crystallization between the case with seed layer and without seed layer.

Generally, a-Si films are deposited at low temperature on the plastic substrate. In our experiment, CeO2 film was grown by rf sputtering using plasma ON/OFF method at the room temperature. Amorphous silicon was deposited by inductively coupled plasma chemical vapor deposition (ICP-CVD) at the room temperature. Then, active layer was crystallized by XeCl excimer laser irradiation. We determined the crystallinity through Fourier Transform Raman spectroscopy (FT-Raman spectroscopy) and Scanning Electron Microscope (SEM) images.

C/P32 STRESS-ASSISTED LATERAL GROWTH OF POLY-GERMANIUM FOR FABRICATION OF THIN-FILM TUNNELING TRANSISTORS ON FLEXIBLE PLASTIC SUBSTRATES

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We report, for the first time, realization of thin film field-effect tunneling transistors made by poly-Ge on flexible PET substrates. Stress-assisted Cu-induced lateral growth of poly-Ge was exploited to fabricate the transistors. Sample preparation was performed by e-beam deposition of a 1000Å a-Ge and a 2000Å SiO2 layer on 100μm-thick PET substrates. After patterning the SiO2 layer, a 100Å Cu layer is deposited by thermal evaporation. The sacrificial oxide is removed by lift-off, leaving the Cu-seeded islands on a-Ge layer. Samples are then subject to thermo-mechanical post-treatment at an annealing temperature of 150˚C and an external compressive strain of 0.05% by inward bending of the substrate. Lateral growth of Ge is possible only in the presence of compressive stress, as confirmed by SEM and TEM analyses, showing grains aligned in the direction of stress. Transistor were fabricated by choosing the drain and source regions as the Cu-seeded areas and depositing a 2000Å SiO2 dielectric and a metal gate over the initially amorphous channel area. Lateral growth of poly-Ge from the drain and source regions, progresses into the channel area with a growth rate of 2.5µm/hr in the direction of the stress axis. A potential barrier is formed in the midway channel where the two lateral growth frontiers meet, possibly due to the lattice mismatch leading to local depleted areas at this location. This barrier formation could by due to tetragonal partial phase transition, as observed by XRD. Carriers need to tunnel this barrier to form the drain-source current. The barrier can be controlled by the gate bias, as confirmed by electrical measurements. An ON/OFF ratio of 10000 shows the potential of these devices for switching applications for flexible display technology.

C/P33-C/P35: Devices

C/P33 LOW TEMPERATURE FABRICATION OF POLY-GERMANIUM TRANSISTORS SUITABLE FOR REALIZATION OF SIMPLE INVERTERS ON FLEXIBLE PET SUBSTRATES

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Fabrication of high-mobility depletion-mode poly-germanium transistors on flexible PET substrates at temperatures as low as 130°C is reported. All deposition steps are carried out at temperatures below 100°C and a base pressure of 10-6 Torr. Sample preparation is started by e-beam evaporation of a 750Å/10Å/750Å thick sandwich layer of a-Ge/Cu/a-Ge on 120um thick PET substrates. Applying external compressive stress to the samples results in a drastic drop in crystallization temperature of Ge-layer from 400°C to 130°C. SEM, XRD, TEM and Raman spectroscopy analyses corroborate the quality of the crystalline Ge film. Active region of transistors are formed by proper patterning of a-Ge layer before thermo-mechanical post-treatment to alleviate the crack formation evolved during the annealing step. Gate insulator and gate metal are then formed by e-beam evaporation of SiO2 and Ni respectively, followed by patterning of the layers. The fabricated Ge-based TFTs are p-type devices. The ID-VGS plot of these transistors shows an On/Off ratio of 40000 and a threshold voltage of 15 Volt. Also a field effect mobility of 110 cm2/Vs is extracted for the poly-Ge layer. These devices are used for low temperature fabrication of inverter circuits consisting of two poly-Ge transistors, combined with poly-Ge resistors on PET substrates. Realization of complementary circuits requires n-type transistors which are not currently possible with Ge TFT's. We are attempting to use silicon-germanium alloys to realize n-type transistors, using the same thermo-mechanical annealing. The crystallization of

SiGe films with 30% Si has been confirmed by TEM and XRD analyses. Fabrication of n-type SiGe thin film transistors for realizing a simple logic circuit on PET substrates is underway.

C/P34 LOW LEAKAGE AND HIGH PERFORMANCE OF NMOSFET USING SiGe LAYER AS A DIFFUSION BARRIER

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As a boron diffusion barrier, SiGe layer was successfully used in n-channel MOSFET using the compatible structure with compressively strained-SiGe p-channel MOSFET, which enables seamless complementary MOS fabrication. The developed n-channel MOSFET has an enhanced gm (12~46%) and nearly unchanged sub-threshold slope under various drain-source voltage in comparison with the devices with standard CMOS device. Especially, in that the enhanced property of sub-threshold slope is one of major concerns in the scaling of MOS devices, i.e., low leakage devices, the usage of SiGe layer as a diffusion barrier at high doped N well in the aggressive device scaling is an excellent candidate in the device fabrication techniques for low power and high performance.

C/P35 FABRICATION OF P-WELL RESONANT TUNNELING DIODE BASED ON SiGe/Si AND ITS DC PARAMETERS EXTRACTION

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In this letter, a p-well SiGe/Si RTD is proposed and demonstrated. I-V relationship is characterized by Keithley 4200 semiconductors parameter analyzer, and negative differential resistance feature is observed clearly at room temperature. The obtained peak current density is 45.9kA/cm2, and peak to valley current ratio PVCR is 2.2.

We use the physics-based I-V equation to extract the DC parameters from the experimental data. It is shown that current I can be separated into two terms: the first term describes mainly the ideal resonant tunneling current denoting by I1，but it cannot reflect the effect of non-elastic scattering on current in the second positive differential conductance region, so the second term must be added, and I=I1+I2. It is found from I-V curve that the bias at peak current is relatively high in this device; we conclude that this is due to the large series resistance (SR) in the contact. We extract the DC parameters of SiGe/Si RTD by considering the effect of SR for the first time in the I-V relationship. Taking into account of this SR, the I-V equation is rewritten to a transcendent equation that we cannot determine the physical parameters directly from curve fitting. In order to simplify the extraction proceeding, the curve is separated into two parts, and V1 at valley current acts as the turning point. Using the data of V³V1，we extract three parameters including SR from I2 while the ideal resonant tunneling current I1 in this region can be neglected. Then the other parameters are extracted form the total current. All the extracted parameters are substituted into the original I-V equation, the resulting fitting curve matches the experimental data quite well, demonstrating the validity of the calculation.

C/P36-C/P44: Optoelectronics

C/P36 PHOTOACTIVE HYBRID POLYMER FOR PHOTONIC WAVE GUIDE APPLICATION

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Organic inorganic polymer have been prepared, characterized and tested for photonic lightwave technology. The photopatternable polymer are consisted of inorganic oxide chain and cross-linked or substituted by organic group. The materials are prepared by solgel process from organosilane and zircone precursors incorporated with organic polymerizable group. The multilayer film were coated by spin or dip technique. The photonic properties of the films such as thickness, surface morphology, refractive index changes and optical loss were characterized by a profiler, scane electronic microscope and photonic prism coupling methodology. A optical planar slab wave guide for infrared region was fabricated and characterized.

C/P37 GROWTH AND OPTICAL PROPERTIES OF ZINC OXIDE THIN FILMS PREPARED BY PLASMA IMMERSION ION IMPLANTATION

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Zinc oxide, which is a wide band gap (3.37 eV at room temperature) semiconductor material, is considered to be a potential material in short wavelength optoelectronic devices such as light-emitting diodes and lasers working in the ultraviolet and blue regions. Zinc oxide thin films can be fabricated using thermal evaporation, metal organic chemical vapor deposition (MOCVD), pulses laser deposition (PLD), molecular beam epitaxy (MBE), and so on. In this work, a dual plasma technique encompassing the use of a zinc cathodic arc plasma and oxygen gas plasma was used in our plasma immersion ion implanter to fabricate Si-based ZnO thin films. Chemically, the ionized zinc atoms and oxygen plasma are easy to bond and the film can be deposited with the proper stoichiometry. Si-based ZnO thin films with different orientations were produced using different substrate bias ranging from -100 to -500 V. The surface morphologies were examined by atomic force microscope (AFM) and the optical properties were investigated by UV-visible absorption spectroscopy and photoluminescence with and without thermal annealing. Using this technology, nitrogen ions were also incorporated into tne ZnO thin films which exhibit interesting properties because nitrogen is believed to be a promising p-type dopant in ZnO.

C/P38 POLYCRYSTALLINE SILICON THIN FILMS MADE BY METAL INDUCED CRYSTALLIZATION FOR SOLAR CELL APPLICATION

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Recently, polycrystalline silicon thin films are attracting more interest in electronic devices such as transistors, solar cells and sensors. In order to crystallize the amorphous silicon film, annealing treatments are conventionally carried out at temperatures in the range 850-1000℃ for a fixed time. However, high crystallization temperature induces the substrates like glass to soften or to get bent. To overcome this problem, metal induced crystallization has been investigated for a long time. Metal like aluminum, nickel, gold, and silver are very much used to decrease the crystallization temperature to below 600℃. When we use metals like tin or indium, the crystallization is possible at temperature as low as 230℃ because of the low eutectic temperature between silicon and these metals. In the case of solar cells, with the crystallization of amorphous silicon at low temperature along with low-cost substrates, it is possible to reduce the costs of the solar cells. In the present work, we prepared the two structures of a-Si/metal/glass and a-Si/metal/n-type Si where the a-Si is crystallized below the eutectic temperature through a rapid thermal process. The as-deposited silicon on the glass substrate was fully crystallized without

amorphous phase under a crystallization time of 10 min. The crystallization was found to increase along the <111> preferential orientation with the increase of the treatment time. In this article, we discuss the crystallization of the silicon thin films by aluminum, tin and indium induced crystallization for the solar cell device application.

C/P39 EFFECT OF PRESSURE ON SURFACE PASSIVATION OF SILICON SOLAR CELL BY FORMING GAS ANNEALING

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Forming Gas Annealing (FGA) of the single crystalline commercial silicon solar cell was carried out at the various conditions of temperature, pressure and gas ratio on different qualities of sample cells. We observed a significant impact of pressure on the performance parameters of the sample cells after the forming gas annealing at some significant pressure. But, the sample cells fabricated in the same condition showed degradation after the forming gas annealing at lower pressure. We basically report in this paper the effect of pressure in the surface passivation mechanism of silicon solar cell by Forming Gas. Also, we present a comparative analysis of the Forming gas annealing at certain pressure and that at vacuum condition. We carried out a series of experiments on the solar cells samples of various sizes and fabrication conditions. The result of our experiment provides guidelines for improving the performance parameters of commercial silicon solar cell by a low cost and easy step of Forming Gas Annealing.

C/P40 EXCLUSION of CHARGE CARRIERS in ELECTRONIC POLYCRYSTALLINE SILICON

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As it is well-known, silicon is the material of choice for reliable and low-cost different applications in nano- and optoelectronics (from integrated circuits (IC) to TFT's and flat-panel displays) Nevertheless, some processes taking place in the polycrystalline silicon samples of finite length, such as carrier exclusion, are of particular interest. As it is known, the carrier exclusion becomes apparent as the following dependence: j~(Va)1/2, where j stands for the current and Va is an applied voltage. Until now processes of carrier exclusion were studied for monocrystalline Si and Ge only. The abstract reports for the first time results of studies carried out on polycrystalline silicon specimens of n-type conductivity at the room temperature in order to clarify effect of the crystal structure on electric field-induced properties. Samples with columnar and grain type of crystal structure were chosen. For simplest non-destructive electric investigations. It was shown that the exclusion of carriers was observed in the samples of columnar crystal structure; at the same time, specimens of grain type structure showed synthetic mechanism: exclusion + tunneling of carriers through intergranular boundaries. The effect of heat treatment of the samples under 9000C and 11000C on described properties was also studied. Experimental results are numerically modeled, and summary of investigations seems to be useful for future applications of polycrystalline silicon.

C/P41 THE STUDY OF THE DENSITY OF LOCALISED GAP STATES IN AMORPHOUS SILICON MATERIAL USING SPACE CHARGE LIMITED CURRENTS TECHNIQUE

S. Guessasma(a),M. Chahdi(b), (a)LERMPS-UTBM, Belfort, France, (a)Semiconductor Characterization Laboratory, Batna University, Algeria

This work deals with the numerical application of the SCLC phenomenon on n+in+ structures of amorphous silicon. The aim was to develop a framework to validate through the j-v characteristic that represent the DOS functions corresponding to genuine effect of disorder in this kind of material. This work permitted to get an insight into the phenomenon involved in its different aspects therefore to state a generalised treatment and recognise different j-v characteristics from a variety of DOS functions.

C/P42 GETTERING BY HEAT THERMAL PROCESSING: APPLICATION IN CRYSTALLINE SILICON SOLAR CELLS

N. Khehdher, A. Ben Gaballah, M. Hassen, M. Hajji, M.F. Boujmil, B. Bessaïs, H. Ezzaouia, R. Bennaceur, Tunisia

Rapid thermal processing (RTP) originally developed for processing microelectronic devices has been investigated in the recent decade for its potential in the production of silicon solar cells. New directions in photovoltaics depend very often on financial possibilities and new equipment. The aim of this study is to present the improvement by gettering treatments by using an infrared lamps heating furnace for removal of metal impurities. Before annealing, the Si substrates is exposing to acid vapors issued from a mixture of HNO3 and HF. This technique surname Chemical Vapor Etching (CVE) method. This technique enables us to groove the Si wafers on the both surface and to realize side buried and rear buried contacts (RBC). This findings show that the CVE process leads to an anisotropic groove which enables us to groove locally and in depth Si wafers using an adequate anti-acid mask. The grooved areas have a sufficient resolution to be applied in Si solar cells. The first step consists in making heat treatment of the sample using a Porous Silicon sacrificial layer on both sides at temperature 1000°C during 60 min annealed time in SiCl4 ambient. The second stage, simultaneous diffusion of phosphorus from a POCl3 source and aluminum layer is used to realize emitter and back surface field in a single high-temperature step, with optimized gettering effect. This CVE - based grooving technique was used to achieve buried grid metallic contacts in order to improve the current collection in Si solar cells, without altering the illuminated surface. A significant enhancement of the current density and the spectral response of the Si cells were observed. The improvements prove the gettering of impurities through the wafer

C/P43 OPTICAL CHARACTERIZATION OF β-FeSi2 LAYERS FORMED BY ION BEAM SYNTHESIS

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Thin β-FeSi2 layers have been prepared by ion beam synthesis (IBS) on (111)Si substrates. The obtained samples have been characterized by means of infrared and Raman spectroscopies. The infrared (IR) transmittance spectra show an absorption at 350 cm-1 as an indication of the initial nucleation of β-FeSi2 precipitates during the implantation of iron into silicon substrate. The main feature of the photoluminescence (PL) measurements performed at 12 K in the β-FeSi2 / (111)Si samples annealed at 850 °C for 90 min is an intense peak localized at 0.811 eV. This peak is assigned to optical radiative transitions intrinsic to β-FeSi2 silicide. Keywords: IR, Raman Spectroscopy, β-FeSi2 , PL

C/P44 SYNTHESIS AND CHARACTERIZATION OF NEW OPAL BASED MATERIALS

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A natural Opal is a package of SiO_2 spheres periodically arranged in such a way that exist a periodic modulation of the refraction index in three dimensions and consequently presents Bragg diffraction in the visible. Opals can be prepared synthetically using the Stobe-Fink-Bohn method[1] which consist of two phases, that is, the hydrolysis of TEOS ($Si(C_2H_5O)_4$)

in ethanol/water and a subsequent condensation where are formed siloxanes (Si-O-Si-O) bonds. In the present work a combinatorial method to get around 100 different opals was used, in order to obtain different sphere diameters.

The analysis of isotherms of physical adsorption of gases and vapors represent a standard and conventional method for obtaining information about the pore structure of porous materials [3-6]. During the last years the standard method for the determination of the Pore Size Distribution (PSD) in the mesoporous range with the help of adsorption isotherms was the Barret-Joyner-Hallenda (BJH) method [3], however this methodology do not estimate properly the PSD [3,5,6]. Recently a new methodology of adsorption isotherm calculation based on the Non-Local Density Function Theory [5-9] which was originated in the Density Functional Theory applied to inhomogeneus fluids [5-9] have revolutionized the methodology of PSD calculation in microporous (less than 2 nm) and mesoporous materials (2 to 50 nm) [3,4]. This methodology has been successfully implemented in the Surface Area and Pore Size Analyzer used in the present study and the first experimental results have been obtained.

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Thursday, May 27, 2004 — Morning

Session VII: High-k dielectrics III
Session chairs: A.J. McKerrow

C-VII.1 08:30 -INVITED-

EPITAXIAL GATE DIELECTRICS: COMPLEX OXIDES TECHNOLOGY TO MEET SILICON'S FUTURE

J. Fompeyrine, G. Norga, C. Marchiori, A. Guiller, D. Halley, J.W. Seo, H. Siegwart, D. Caimi, D.J. Webb, C. Rossel, R. Germann and J.-P. Locquet, IBM Research Division, Zurich Lab, Saeumerstr. 4, 8803 Rueschlikon, Switzerland

Crystalline oxides grown epitaxially on silicon may provide a path towards gate dielectrics with very low equivalent oxide thicknesses (EOT<0.5nm). Nevertheless, they could allow device engineers to not compromise on power consumption and keep gate leakage at low levels. This unique combination derives from their intrinsically higher k. A substantially greater physical thickness can be afforded with respect to amorphous high-k. Clearly, this first objective can only be reached if the formation of an amorphous low-k interfacial phase is kept under tight control. Any interfacial monolayers will increase the EOT by more than 20% for such low EOT ranges. In light of this objective, the latest development in this field have been done following five complementary approaches: (1) materials selection guided by bulk thermodynamics; (2) interface thermodynamics; (3) structural matching of the silicon and epitaxial oxide lattices; (4) oxidation kinetic control during all process stages and (5) development of process-specific tools. The aim of this talk is to prove that deposition processes can be developed with an appropriate combination of these five cornerstones. It allowed us to control the transition from silicon to a crystalline oxide layer, using perovskites Sr(Ti,Zr)O3 or pyrochlores La(Zr,Hf)O3.5 Together with the development of a specific MBE deposition tool, we will then show that our initial objective has been reached.

C-VII.2 09:10

A GRAZING INCIDENCE X-RAY DIFFRACTION STUDY OF ULTRA-THIN PRASEODYMIUM OXIDE LAYERS ON Si(001): FROM PSEUDOMORPHISM TO BULK BEHAVIOUR

Thomas Schroeder, Tien Lin Lee, Laure Libralesso and Jörg Zegenhagen, E.S.R.F., Beamline ID 32, 6, Rue Jules Horowitz, 38043 Grenoble, France, Christian Wenger, Peter Zaumseil and H.-J. Müssig IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Ultra-thin heteroepitaxial praseodymium oxide films on Si(001) show promising results for future applications in microelectronics devices. To optimize the materials properties of this functional oxide / semiconductor system, the key parameters of the growth process must be accurately understood. For this purpose, a Synchrotron Radiation - Grazing Incidence X-Ray Diffraction (SR-GIXRD)study was applied to determine the film morphology over the technologically important thickness range (1-10 nm). Praseodymium oxide films grow with the rectangular (101) crystal face of the cubic oxide phase (space group: Ia3) on Si(001). The high-symmetry in-plane directions of the oxide face are oriented along the Si(110) azimuthes so that the in-plane lattice parameters of the oxide and the Si substrate match within three percent. This lattice mismatch causes a compressive strain along the oxide [010] and a tensile strain along the oxide [10-1] in-plane direction, resulting in a distortion of the oxide film in the pseudomorphic regime (<4nm). Studying various film thicknesses in the range from 1 to 10 nm allowed to monitor the evolution of the oxide lattice parameters under this complicated strain field from almost perfect pseudomorphism to pure bulk-like behaviour. The X-ray data is supplemented by STM studies which focussed on the submonolayer coverage regime.

09:30 **BREAK**

Session VIII: Atomic layer growth
Session chairs: A. Paccagnella

C-VIII.1 09:40 -INVITED-

MOCVD BASED DEPOSITION TECHNOLOGIES FOR ATOMIC LEVEL GROWTH OF NEW MATERIALS AND THE CHALLENGES FOR THEIR INTRODUCTION INTO MAIN STREAM SEMICONDUCTOR DEVICES

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Today the silicon industry has reached a point where further shrinking of CMOS devices sees the “red brick wall” in closer proximity and most likely it never has been reached a point in the past, where such a tremendous amount of potential material candidates are being discussed as potential material solution in highly integrated main stream semiconductor devices.

Therefore, alternative high-k gate dielectrics, electrode materials and specifically their processing methods have become increasingly important to enable further CMOS scaling, following Moore’s law of rapid performance doubling. Integrating new materials into a standard CMOS device flow raises many challenges with regard to the compatibility with the silicon surface itself especially if the physical film thickness has to be decreased to the limits in order to facilitate potential for further device shrinking in the future. Interface related effects and consequently film formation processes during growth of the layers become key objectives mandatory to be understood. This paper gives an overview about MOCVD based processes in comparison to ALD type deposition modes. In particular a pulsed MOCVD type of approach will be presented and discussed based on dielectric and conductive materials like HfO2, Pr2O3 Ru, RuO2 and others. Influence of process conditions and precursor materials on electrical and morphological properties of these films will be discussed in the light of the potential use of these materials in next generations of semiconductor devices.

C-VIII.2 10:20

INFLUENCE OF OXYGEN PRECURSORS (H2O or O3) ON THE PROPERTIES OF AS GROWN AND ANNEALED HfO2 FILMS GROWN BY ATOMIC LAYER DEPOSITION FROM HfCl4, Hf(mmp)4, AND Hf(OtBu)2(mmp)2

G. Scarel, C. Wiemer, S. Spiga, G. Tallarida, S. Baldovino, E. Bonera, S. Ferrari and M. Fanciulli
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HfO2 is among the most promising candidates to substitute SiO2 as active dielectric in CMOS devices. ALD is a very suitable growth technique, but precursors and growth parameters need to be optimized. We report on the properties of HfO2 film grown using H2O and O3, and HfCl4, Hf(mmp)4, and Hf(OtBu)2(mmp)2 as Hf sources. Hf(mmp)4 and Hf(OtBu)2(mmp)2 are new volatile, mononuclear and precursors, weakly sensitive to air, reactive enough to oxidizing agents at the growth temperatures of interest for ALD. The analyzed films on Si(100) are 5 to 30 nm thick and are annealed in N2. At 375 C, H2O and O3 combined with HfCl4 generate HfO2 films in a mixture of monoclinic and orthorhombic phases. Films deposited using Hf(OtBu)2(mmp)2 are generally less dense and with a higher content of monoclinic phase. O3 however promotes films with lower roughness, slightly higher growth rate, higher electronic density, less Cl, F, (OH)-, and C than films grown with H2O. O3 develops an interface layer thicker than the one developed using H2O. These results can be explained with the different growth mechanism involved when O3 or H2O are used as oxygen precursors. Indeed, differently than H2O, O3 rules out (OH)- and is efficient only above 250 C. Decomposition of the metallorganic precursors can heavily affect film structural and morphological properties. MIS capacitors are fabricated by Al thermal evaporation through a shadow mask for C-V and I-V measurements. The dielectric constant k determined from the accumulation capacitance does not significantly depend on the various precursor combinations, but on film thickness (k decreases from 15 to 11). Films grown from HfCl4 + H2O show the lowest hysteresis and interface state density. Interface defects are investigated.

10:40 **BREAK**

Session IX: Front End of Line I
Session chairs: M. Specht

C-IX.1 11:00 -INVITED-

UNDERSTANDING AND MODELLING BORON DEACTIVATION / ACTIVATION IN LOW-RESISTANCE ION-IMPLANTED ULTRASHALLOW JUNCTIONS

N.E.B. Cowern, B. Colombeau, A.J. Smith, K. Kirkby, Advanced Technology Institute, University of Surrey, Guildford GU2 7XH, U.K., B. Pawlak, R. Duffy, Philips Research Leuven, Kapeldreef 75, 2001 Leuven, Belgium, S.B. Felch, H. Graoui, A. Mayur, M.A. Foad, Front End Products, Applied Materials Inc., 974 E. Arques Avenue, Sunnyvale CA 94086, USA and N. Zographos, C. Zechner, ISE Integrated Systems Engineering, Balgriststrasse 102, 8008 Zürich, Switzerland

In order to continue scaling p-channel MOS transistor transconductance into the range of gate lengths below 50 nm, the semiconductor industry needs to find ways to introduce boron concentrations approaching $10^{21}/cm^3$, far above the equilibrium chemical solubility limit reached by conventional implantation and thermal processing. The talk considers how this can be achieved using ion-implanted source-drain structures, taking into account the physical mechanisms of boron deactivation and activation that occur during thermal processing. We consider two promising technologies at opposite ends of the thermal energy spectrum: (i) solid-phase epitaxial regrowth at low temperatures, (ii) ultra-short time high temperature processing. Despite major differences in terms of engineering, in both cases boron activation and thermal stability are regulated by the same atomic-scale interactions between dopants, point defects and extended defects that evolve during thermal processing. Quantitative modelling of boron source-drain evolution, based on these atomistic phenomena, will be presented. It provides an excellent description of experimental observations on source-drain deactivation and activation, and offers a coherent basis for future decisions on source-drain processing technology.

C-IX.2 11:40

TEMPERATURE SCALING FOR 35 NM GATE LENGTH HIGH-PERFORMANCE CMOS

Th. Feudel, M. Horstmann, M.G erhardt, M. Herden, L. Herrmann, D. Gehre, Ch. Krueger, D. Greenlaw and M. Raab, AMD Saxony LLC & Co. KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Germany

It is commonly assumed that reducing the source-drain extension (SDE) junction depth is a key element for next-generation technology nodes. This can either be achieved by reducing the implantation energy or by reducing the thermal budget of the annealing process.

In this paper we will demonstrate that for transistors with an optimum balance between AC and DC performance a reduction in junction depth results only in very little improvement of the short-channel behavior for spike anneals in the temperature range between 1050 and 1130 oC. On the other hand, reduced temperatures, amongst other impact parameters like pattern density and RTA tool design, allow a reduction in in-die parameter variation and improved product performance. There exists an optimum temperature for the compromise between reduced parameter variation and reduced dopant activation. For improved threshold voltage roll-off we introduced super-strong low-energy halos, thus supporting a physical gate length of 35 nm. The problem of increased drain resistance due to reduced activation at lower temperatures and counter-doping with high halo implant doses could be solved by optimizing the lateral diffusion of the deep source-drain areas and by high cool-down rates of the spike annealing process. All electrical data have been extracted from our triple-spacer transistor architecture, manufactured in a 90-nm production technology. An outlook will be given for alternative device concepts, such as SPE anneal and asymmetric devices.

12:00 **LUNCH**

Thursday, May 27, 2004 — Afternoon

Session X: Front End of Line II
Session chairs: N.E.B. Cowern

C-X.1 14:00

DETECTION OF N INCORPORATION IN NM-THIN HFO2 LAYERS ON (100)Si BY ELECTRON SPIN RESONANCE

A. Stesmans and V. Afanas'ev, Department of Physics, University of Leuven, 3001 Leuven, Belgium and F. Chen and S.A. Campbell, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, USA

Currently, HfO_2 and its silicates ($HfSi_xO_y$) enjoy much attention as promising layers of high dielectric constant κ for replacement of conventional SiO_2 as gate dielectric in future complementary metal-oxide-semiconductor (CMOS) devices. Their success in technologically hinges critically on the control of the structural imperfections (defects) of either extrinsic or intrinsic origin left in the high-k layers. To address their atomic nature, a low temperature electron spin resonance (ESR) study has been performed on (100)Si/HfO_2 structures with ultrathin oxide layers deposited by three variants of the chemical vapor deposition (CVD) technique using chemically different precursors. After ^{60}Co γ-irradiation, this reveals incorporation of N in (100)Si/HfO_2 structures with a-HfO_2 films deposited using $Hf(NO_3)_4$ as precursor, through detection of NO_2 radicals, in densities /55 at. ppm. Temperature dependent measurements indicate that the molecules, which are likely homogeneously distributed, are stabilized in the a-HfO_2 network. Based on symmetry considerations, the neutral $N \equiv O_3$ network entity is suggested as precursor, transformed into ESR-active NO_2 upon γ-irradiation. The interesting N incorporation into the HfO_2 network appears inherent to the particular nitrado CVD process, and when N introduced in appropriate amounts, may appear as a beneficial aspect electrically.

C-X.2 14:20

COMPATIBILITY OF ORGANIC LAYERS GRAFTED ON SILICON WITH MICROELECTRONICS

A. Faucheux(a,b), J.-N. Chazalviel(a), F. Ozanam(a), (a)LPMC, CNRS-Ecole Polytechnique, 91128 Palaiseau Cedex, France, (b)STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France

Deposition of high-k oxides on silicon unavoidably results in the presence of an interfacial SiO2 layer. In order to remedy this problem, a covalently grafted organic monolayer on silicon could be used as an ultrathin buffer layer between silicon and the oxide layer.

Here, organic monolayers were prepared by a photochemical hydrosilylation reaction between a hydrogenated silicon surface and alkenes. The thermal stability of such monolayers has been analyzed in order to know whether they can withstand the subsequent fabrication steps of electronic components. This was investigated by means of Fourier Transform Infrared Spectroscopy (FTIR), in the Attenuated Total Reflection geometry (ATR), which provides enhanced sensitivity. A cell was home built to enable the in-situ infrared monitoring of the monolayers in different conditions (temperature, oxidizing or reducing atmosphere). The first results show that the alkyl monolayers remain intact up to 220°C, under air or reducing atmosphere. Above this temperature, they start to decompose. The maximum degradation rate is observed at 250-300°C, depending on the alkyl chains. The details of the experiments will be described and the decomposition process will be discussed.

C-X.3 14:40

ULTRATHIN HfO2 GATE DIELECTRIC ON PARTIALLY STRAIN COMPENSATED SiGeC/Si HETEROSTRUCTURES

S.K. Ray, R. Mahapatra, S. Maikap and A. Dhar, Department of Physics & Meteorology IIT Kharagpur 721 302, India

Alloys of band gap and strain engineered Si1-x-yGexCy has recently become attractive for high performance Si-based heterostructure device applications. However, the growth of good quality ultrathin gate oxides with low interface state density for fabrication of submicron MOSFET devices is still a critical issue. Hafnium oxide seems to be one of the most promising gate materials, combining their high dielectric constant with low leakage current due to a reasonably high barrier height for electron tunneling. The electrical characteristics of ultra-thin HfO2 gate dielectrics deposited on strain compensated Si0.69Ge0.3C0.01 layers by RF magnetron sputtering are presented here. The micro-structural characteristics of the dielectric/SiGeC interfaces were studied by high-resolution transmission electron microscopy showing the absence of any Ge segregation and C pecipation. Electrical characterization was done using fabricated Al-gate MOS capacitors. High frequency C-V and G-V characteristics were used to extract the equivalent oxide thickness, dielectric constant and interface state density. The charge trapping properties of the HfO2 films were studied using Fowler-Nordheim constant current stressing through the gate electrode. An extremely low leakage current density of ~1 x10-7 A/cm2 at a gate voltage of –1.0 V and moderate interface state density of 5.3 x 1011 cm-2 eV-1 were observed with an equivalent oxide thickness of 2.7 nm. The dielectric film exhibited hole trapping behavior under Fowler-Nordheim constant current stressing.

C-X.4 15:00

MICROSTRUCTURE INVESTIGATION OF BaxSr1-xTiO3 THIN FILM GROWN ON POROUS SILICON SUBSTRATE

Weili Liu(a,c), Su Xing(a), J. Lian(b), Lumin Wang(b), Zhitang Song(a), Chenglu Lin(a) and Paul K. Chu(c), (a)Research Center of Semiconductor Functional Thin Film Engineering & Technology, State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, 200050 Shanghai, China, (b)Department of Nuclear Engineering and Radiological Sciences, College of Engineering, University of Michigan, Am Arbor MI 48109-2104, USA, (c)Department of Physics and Materials Science, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon, Hong Kong

Presently there is a significant interest in thin films of ferroelectric barium strontium titanate (BST) because of its unique combination of high dielectric constant, low dielectric loss, low leakage current density, and

good thermal stability. In addition, the dielectric constant of perovskite BST is dependent on electric field, so it is suitable for tunable microwave circuits. In order to be compatible with standard silicon-based ultra-large-scale integration (ULSI) technology, it should be better to fabricate devices on silicon wafers. However, silicon is not a good substrate for microwave components because of its high cross talk. In this paper, porous silicon was employed as the substrate because porous silicon can provide a low substrate loss and low coupling effect due to its high resistivity compared to bulk Si. Thin BaxSr1-xTiO3 (BST) films were fabricated on porous silicon substrate by pulsed laser deposition for the first time. The detailed microstructure of the BST on porous silicon was investigated by X-ray diffraction spectra, atomic force microscopy (AFM), scanning electronic microscopy (SEM) and high-resolution transmission electronic microscopy (HRTEM). Results show that BST films with good quality were grown on porous silicon and the microstructure of porous silicon substrate will affect the size distribution of the grains in the BST film. The interface structure between the BST and porous silicon was also studied by HRTEM and EDS. Results show that the amorphous BST layer in the interface between the crystalline BST and substrate is caused by the diffusion of silicon from the porous silicon to BST.

C-X.5 15:20

MOSFET DRAIN CURRENT REDUCTION UNDER FOWLER-NORDHEIM AND CHANNEL HOT CARRIER INJECTION BEFORE GATE OXIDE BREAKDOWN

S. Gerardin(a), A. Cester(a,b), A. Paccagnella(a,b), G. Ghidini(c), (a)DEI – Università di Padova, via Gradenigo 6B, 35131 Padova, Italy, (c)INFM, Sezione di Padova, via Marzolo 8, 35131 Padova, Italy, (c)ST Microelectronics, via Olivetti 2, 20041 Agrate Brianza, Italy

We studied the degradation of MOSFETs with 2.8nm and 2.5nm gate oxide under Fowler-Nordheim and channel hot electron injection, focusing on the evolution of the characteristics before the occurrence of any oxide breakdown, soft or hard. In order to assess the damage and understand its origin, we monitored different parameters: transfer and output characteristics, gate leakage, charge pumping current, and low frequency noise.

After both types of stress, the MOSFETs showed a substantial drop of the transconductance accompanied by a moderate increase of the threshold voltage. Their combined effect was visible as a substantial reduction of the drain saturation current. At the same time we observed the increase of the gate leakage current (SILC), of the charge pumping current, and of the 1/f noise. In the channel hot carrier stress, the localized nature of the damage on the drain side was clearly emphasized by the steep drop of the output resistance in the saturation regime. We interpreted these results in terms of slow and fast interface-trap creation in the gate oxide, highlighting the correlation between the defects responsible for the different degradations observed. In particular we linked the SILC generation to the low frequency noise increase. Finally we tried to recover the damage by injecting electrons across the oxide at moderate field, reducing only SILC and 1/f noise in this way.

C-X.6 15:40

ANTICIPATION OF OXYNITRIDE ELECTRICAL THICKNESS BASED ON XPS MEASUREMENT

J. Bienacel(a), D. Barge(b), M. Bidaud(b), N. Emonet(a), D. Roy(a), I. Pouilloux(b), K. Barla(a), (a)ST Microelectronics, 850 rue Jean Monnet, 38926 Crolles, France, (b)Phillips R&D Crolles, 850 rue Jean Monnet, 38926 Crolles, France

The downscaling of the CMOS below 90 nm node requires gate oxide with a sophisticated stack to meet both leakage and CET requirement. Although High-K materials offer an attractive solution, they are not ready for industrial integration. Plasma nitridation of a thermally-grown oxide film offers a good compromise for the electrical requirement of the 65nm node.

As the final result is very sensitive to both physical thickness and nitrogen dose, it is highly desirable to predict the electrical properties of such films. The purpose of this paper is to present a simple physical model to forecast the capacitance equivalent thickness (CET). The model is based on total nitrogen dose and dielectric physical thickness, both given by in-line X-Ray Photoelectron Spectroscopy measurement. It includes an estimation of the gate oxide dielectric constant, of the gate depletion capacitance, and of the substrate "dark space" capacitance, based on simple physical hypothesis. Good correlations are obtained between calculated and measured CET, for nitrided oxide from 19Å to 30Å CET and for a large range of incorporated nitrogen doses (1.1015 at/cm^2 to 6.1015 at/cm^2). Modelisations where done on thermally nitrided oxide, as well as on plasma nitrided oxide, with an accuracy of ~0.5Å. This model allows accurate estimation of the CET, whatever the thickness, the nitrogen dose and the process.

16:00 **BREAK**

16:30 **POSTER SESSION II**

see poster session I Wednesday afternoon

Friday, May 28, 2004 Morning

Session XI: Back End of Line I
Session chairs: S. Deleonibus

C-XI.1 08:30 -INVITED- SELECTED CHALLENGES OF ADVANCED INTERCONNECT SYSTEMS

T. Gessner(a,b) and S.E. Schulz(a), TU Chemnitz, Center for Microtechnologies(a); FhG-IZM, Department Micro Devices and Equipment(b), Chemnitz, Germany

Based on the international Semiconductor Roadmap CMOS-based technologies will be continued for the next 15 years. To fulfill speed, reliability and scaling down issues of future devices the interconnect systems have to be modified in terms of metal as well as intermetal dielectric material and their processing.

Within this paper an overview about selected challenges of advanced interconnect systems will be discussed. This includes a comparison of Copper and low k material approaches and optical interconnect concepts. More in detail some scaling approaches of CVD/PVD with respect to the deposition of ultra thin barriers and the application of ultra low k materials will be described. Finally some electro-thermal issues of the low k material integration will be discussed.

C-XI.2 09:10 METALORGANIC CHEMICAL VAPOR DEPOSITION OF SILVER THIN FILMS BY DIRECT LIQUID INJECTION SYSTEM FOR FUTURE INTERCONNECTS

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Typical feature sizes in integrated circuits (ICs) are predicted to shrink rapidly in the next several years, according to the International Technology Roadmap of Semiconductors. In order to decrease resistance, next to copper, silver appears as the most promising material. It has been shown that sputtered silver lines can be scaled down to small feature sizes (film thickness < 100 nm) without a significant decrease in conductivity. Among various Ag film deposition techniques, CVD has the advantage of superior step coverage for high aspect ratio vias and trenches, making it a promising technique of Ag film deposition for future applications. Deposition of Ag films with direct liquid injection-metal organic chemical vapor deposition (DLI-MOCVD) was chosen because this delivery method allows precise control of precursor flow and prevents early decomposition of the precursor as compared to the bubbler-delivery. Silver(I) -2,2-dimethyl-6,6,7,7,8,8,8-heptafluoro-3,5-octanedionato Triethylphosphine [Ag(fod)(PEt3)] as the precursor was studied, which is liquid at room temperature. Ag films were grown on different substrates of SiO2/Si and TiN/Si. Argon and Nitrogen/Hydrogen carrier gas was used in a cold wall reactor at a pressure of 0.5-5 mbar with deposition temperature ranging between 220 to 350 0C. Ag films deposited on a TiN diffusion barrier layer have favorable properties over films deposited on SiO2/Si substrate. At lower temperature (220 0C), film growth is essentially reaction-limited on SiO2 substrate. Significant dependence of the surface morphology on the deposition conditions existed in our experiments. According to XPS analysis pure Ag films are deposited by DLI-MOCVD at 250 0C by using Argon as carrier gas.

09:30 **BREAK**

Session XII: Back End of Line II
Session chairs: G. Ghibaudo

C-XII.1 09:40 -INVITED- ANALYSES OF INTERFACIAL REACTIONS AT DIFFERENT LEVELS OF INTERCONNECTION

T. Laurila and J.K. Kivilahti, Lab. of Electronics Production Technology, Helsinki University of Technology, P.O. Box 3000, 02015 HUT, Finland

Continuous miniaturization of electronic devices increases the importance of the understanding and control of the physical and chemical compatibility between dissimilar materials in order to design and fabricate reliable products. Thermodynamic and kinetic modelling together with careful experimental work is of great help for understanding and controlling interdiffusion and chemical reactions in interconnection structures. The approach provides useful information on the stabilities of phases (microstructures), driving forces for chemical reactions and growth rates of reaction products occurring in interconnections or thin film structures during processing, testing and in long-term use of electronic devices. In this paper two examples of the approach outlined above are presented. Firstly, the case of TaC diffusion barrier between Cu and Si at the IC-interconnection level is discussed. Complex reactions occur in this system especially when oxygen is present as an impurity. Evaluated Si-Ta-Cu, Ta-C-O and Si-Ta-C ternary stable as well as metastable phase diagrams are used together with the calculated activity diagrams and detailed transmission electron microscopy (TEM) results to rationalize the formation of the observed microstructure after extensive reactions. Secondly, reactions occurring between the Al/TiW/Ni/Au under bump metallurgy (UBM) and copper containing lead-free solders at the component side of the solder interconnection are presented. To understand the formation (Cu,Ni)6Sn5 instead of the expected Ni3Sn4 during soldering the ternary Sn-Cu-Ni phase diagram is used. The influence of the subsequent solid state annealing and the related mass-supply effects on the stability of the microstructure are also discussed.

C-XII.2 10:20 MECHANICAL STRESS IN PECVD a-SiC:H: AGING AND PLASMA TREATMENTS EFFECTS

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Hydrogenated amorphous silicon carbide (a-SiC:H) deposited by PECVD is one of the most promising dielectric diffusion barrier available in Cu - Ultra low k interconnections due to its low dielectric constant and

good barrier ability. In these PECVD dielectrics, the mechanical stress is a critical parameter. Many works have demonstrated that water absorption by thin films changes the mechanical stress toward compression. This phenomenon is well known for silicon dioxide films and lead to a drift of the mechanical stress with time during the film storage in the atmosphere. But, few works are devoted to the study of the stress variation upon aging for a-SiC:H. In this work, the mechanical stress evolution with time of a-SiC:H film exposed to room atmosphere is studied and compared with the behavior observed on other PECVD dielectrics (SiN, SiO2, SiCN). For as-deposited a-SiC:H samples, a strong stress evolution with time toward compression is observed and the results are interpreted using a model consisting of three driving forces (surface reactivity, silanol buildup and water dipole interaction). Infrared spectroscopy analysis allows to confirm that the residual stress and OH contents are linked. An oxidation of the hydrogenated amorphous silicon carbide film with time is also observed. Different plasma treatments (He, O2 or H2) have been tested on a-SiC:H films to limit the stress drift with time. Each plasma treatments are able to limit the stress evolution of a-SiC:H films but the mechanisms are different in each cases : densification of the film with He plasma treatment, formation of a dense oxide at the surface with O2 plasma treatment and passivation of dangling bonds with H2 plasma treatment.

10:40 **BREAK**

Session XIII: Back End of Line III
Session chairs: M. Schumacher

C-XIII.1 11:00 -INVITED- LOW-K MATERIALS AS A SUBSTITUTE FOR TRADITIONAL BEOL DIELECTRICS

Andrew J. McKerrow, Silicon Technology Development, Texas Instruments Inc., Dallas TX 75243, USA

With increasing demands on interconnect performance the semiconductor industry is replacing traditional BEOL dielectrics with materials characterized by a lower dielectric constant. At the 90 nm technology node this includes replacement of the SiO_2 or FSG intermetal dielectric (IMD) with materials characterized by a dielectric constant of k = 2.8-3.0. Further improvements in interconnect performance are also realized by replacing silicon nitride (SiN) dielectric barriers/etch stops with a lower k material. Development activities at the 65 nm technology node, and beyond, are focusing on extending materials solutions identified at the 90 nm node through further reduction in dielectric constant.

Organosilicate glasses (OSGs) are one class of materials that are qualified at several semiconductor companies as intermetal dielectrics at the 90 nm node. This class of materials typically have a chemical composition of $SiO_x(CH_3)_yH_z$ where x:y:z vary depending on processing conditions. OSGs can be conceptualized as a silicon dioxide in which some oxygen atoms are replaced by methyl (CH_3) functional groups. It is believed that the lower dielectric constant of OSGs result from the combined effects of reduced polarization of the Si-C bond and a reduction in density. Materials of this class should be extendable beyond the 90 nm technology node through incorporation of porosity in dielectrics with a similar $SiO_x(CH_3)_yH_z$ skeleton.

In this presentation we will review deposition and chemical composition of OSGs. The material properties of OSGs will be compared and contrasted to denser SiO_2 thin films with particular attention paid to the effects of moisture on film stacks incorporating OSGs. Specifically, as these dielectrics have a tensile biaxial stress they are prone to stress corrosion cracking, a phenomenon in which crack growth is affected by the chemical environment near the crack tip. This phenomenon is well understood for bulk glasses and recently we observed similar behavior in OSG thin films that were capped with TEOS, SiN, or TaN. These results will be reviewed as well as recent studies of the diffusion of water in low-k materials.

Replacement of SiN dielectric barriers/etch stops with materials of a lower dielectric constant afford another possible means of improving interconnect performance. PE-CVD deposited silicon carbide (SiC) films containing oxygen (SiCO) or nitrogen (SiCN) are candidates to replace SiN. The dielectric constant of SiCO & SiCN thin films span a range from 4.5 to 5.5, compared to ~ 7.0 for SiN, but their successful integration hinges on establishing comparable reliability to SiN.

In this presentation we will summarize our studies of SiCO, SiCN, and SiN thin films that were integrated in a dual-level metal copper-OSG interconnect. Data from Voltage Ramp and TDDB testing of comb/serpent test structures will be presented indicating that thermally-activated changes in SiCO electrical performance may be indicative of the film's poor moisture-blocking properties. In comparison, SiCN films will be shown to be characterized by dielectric properties that more closely resembled those of SiN.

C-XIII.2 11:40 POROUS EXTREME LOW K (ELK) DIELECTRICS USING A PECVD POROGEN APPROACH

L. Favennec(a), V. Jousseaume(b), V. Rouessac(c), F. Fusalba(a), J. Durand(c)and G. Passemard(a), (a)STMicroelectronics 850 rue Jean Monnet, 38920 Crolles, France, (b)CEA/Leti 17 rue des Martyrs, 38054 Grenoble Cedex 9, France, (c) Institut Européen des Membranes /UM 2-CC047 Place Eugène Bataillon 34095 Montpellier Cedex 5, France

The introduction of new dielectrics into Si chip interconnection technology, to improve the electrical performance of ULSI, is marked by continuous revisions to meet the ITRS projection. Amorphous SiOC:H (K=2.9) deposited by PECVD from linear precursors is now in scale up towards production. Using other precursors like cyclic siloxanes, K value is reduced to 2.5 at least. However, sub-65nm technologies need K values below 2.5 and an extendable material to further decrease K values. The main way to reduce the dielectric constant is to introduce porosity into the film. In this work, a two steps porogen approach is followed to perform ELK (K<2.5) deposition. Firstly a dual-phase thin film is deposited by PECVD using two advanced precursors : decamethyl-penta-siloxane (D5) and a sacrificial organic precursor. Short chain siloxanes are generally employed to create an a-SiOC:H based matrix. In this study, D5 and plasma parameters were chosen to minimize the matrix density, i.e. to get a cyclic plasma-polymer matrix. Within this matrix, the organic precursor creates organic inclusions. In a second step, the organic molecules are removed by a suitable curing to generate porosity. Various types of organic precursors and post treatments are investigated and thin films are then fully characterized. Incorporation and removal of organic molecules

from a-SiOC:H material are closely studied using infrared spectra. K value of the deposited porous dielectric was measured at 2.3, using a Hg probe. Nitrogen adsorption isotherms measurements prove the material porosity confirmed by a reduced density, controlled by XRR. This work clearly demonstrates the ability of achieving an ELK with a PECVD porogen approach using D5 as matrix and new organic precursors as porogen.

12:00 **LUNCH**

Friday, May 28, 2004 Afternoon

Session XIV: Materials challenges processes and materials II
Session chairs: T. Gessner

C-XIV.1 14:00

EXPANDING THERMAL PLASMA FOR LOW-K DIELECTRICS: ENGINEERING THE FILM CHEMISTRY BY MEANS OF SPECIFIC DISSOCIATION PATHS IN THE PLASMA

M. Creatore, W.M.M. Kessels, Y. Barrell, M.C.M. van de Sanden, Department of Applied Physics, Eindhoven University of Technology, Den Dolech 2, 5600 MB Eindhoven, The Netherlands

As the need for low-k dielectrics in the ULSI technology becomes urgent, the research focuses on the deposition of novel materials with appropriate electrical properties and on the challenges concerning their integration with subsequent processing steps. Here we address the remote expanding thermal plasma as a novel technique for the deposition of low-k carbon-doped SiO2 films from Ar/hexamethyldisiloxane (HMDSO)/oxygen mixtures. Film characterization has been obtained by means of IR absorption spectroscopy and UV-VIS ellipsometry. These results have been correlated with capacitance (at 1 MHz) and nano-indentation measurements. We have obtained films with k values in the range 2.9-3.4 and still fairly good mechanical properties (hardness 1 GPa, Young’s modulus 10 GPa). This outcome is surprising because literature, in general, reports on low-k films deposited from precursors with 2 Si-O and 1 Si-C bonds per Si atom (e.g., diethoxymethylsilane), in order to reach a compromise between dielectric and mechanical film properties. Our approach, on the contrary, utilizes HMDSO, characterized by a relatively high Si-CH3: Si-O bond ratio. The plasma chemistry investigation by means of Cavity Ring Down Spectroscopy and Mass Spectrometry has highlighted that the HMDSO molecule preferably dissociates at the Si-O bond. In this way, the loss of Si(CH3)3 radicals is expected to account for the major removal of CH3 groups from the chemistry of the deposition precursors. A careful identification of the deposition precursors is not only functional in controlling the carbon presence in the film and, therefore, the quality of the low-k dielectric, but it is also expected to pave the way towards the engineering of ultra-low-k materials.

C-XIV.2 14:20

DEPTH PROFILED POROSITY AND MICRO-STRUCTURE EVOLUTION STUDIED BY POSITRON ANNIHILATION AND RAMAN SPECTROSCOPY IN SIOCH LOW-K FILMS

C. Macchi, G. Mariotto, A. Zecca, M. Bettonte and R.S. Brusa, Dipartimento di Fisica, Università di Trento and INFM, 38050 Povo (TN), Italy

The 3γ annihilation of ortho-positronium and the Doppler broadening of the positron annihilation line have been measured by implanting low energy positrons in low dielectric constant (low-*k*) SiOCH films. Positron techniques were used to detect the porosity while Raman scattering was employed to study the microstructure of the films. The evolution of the film porosity and of the microstructure was followed as a function of the thermal treatments in the 400–900 °C temperature range. The films have been produced by plasma enhanced chemical vapor deposition (PECVD) and after annealing in N_2 atmospheres at 400 °C have been treated in N_2+He plasma. The treatment in the N_2 plasma was found to seal the pores in the first 45 nanometers. The minimum free volume of the pores in the as-produced samples has been estimated. The chemical environments of the pores probed by positrons were found to be stable up to 600 °C thermal treatment. At 700-900 °C annealing temperature a reduction of the hydrogen content and a change in the chemical environment of the pores has been observed. Raman spectroscopy indicates the formation of carbon nanostructures at these temperatures.

C-XIV.3 14:40

NITROREN DOPED SILICON: PROSPECTS FOR PERFECT MATERIAL DESIGN

V.G. Litovchenko, A.A. Efremov, A.V. Sarikov, Institute of Semiconductor Physics, 45 Nauki av., Kiev 03028, Ukraine and H. Richter, IHP/BTU Joint Lab, Universitatsplatz 3-4, 03044 Cottbus, Germany

Nitrogen doped silicon is presently one of the intensively studied candidates to replace ordinary CZ silicon in future microelectronics, especially in the case of ultra--large diameter wafers. The most attractive features of N-Si are higher resistance to the point defects agglomeration and easier nucleation of SiO2 precipitates. All this allows us to hope to obtain more perfect material: mesoscopically homogeneous and unstressed. The present paper is devoted to experimental (IR-LST) and theoretical study of mutual influence of nitrogen and oxygen during SiO2 precipitation. Unusual kinetics of precipitation, nucleation and growth results in two-humped distribution function of precipitates over size. Computer simulations have shown that two types of nucleation centers cause such behavior: permanent ones related to native structural defects, and dynamically formed centers generated in reactions with nitrogen. On the other hand, it was found that nitrogen itself activates nucleation even at native defects, and is simultaneously absorbed by growing nuclei. The ways to use these multiple feedbacks for optimizing control of material properties are discussed.

C-XIV.4 15:00

SIMULTANEOUS OPTICAL MEASUREMENT OF GE CONTENT AND BORON DOPING IN STRAINED EPITAXIAL SIGE FILMS USING A NOVEL DATA-ANALYSIS TECHNIQUE

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We here present a novel technique, based on a proprietary approach to analyzing the raw optical data, which is able to decouple the effects of Ge and B on the optical properties of a B-doped SiGe film and so measure the two material fractions, plus the thickness, simultaneously and independently on a standard Opti-Probe® film-thickness tool.

Two sets of doped epitaxial SiGe layers were grown, each with a nominally fixed Ge-content but with the Boron levels varying from zero to ~1E20cm^{-3}. One set consisted of single-layer films on c-Si substrates, the other consisted of similar films capped with undoped epi-Si layers.

In each case, the Ge-fraction found was in good agreement with expectation (and with XRD for the undoped sample) whilst the calculated "doping parameter" was found to follow a monotonic relationship with changes in Boron concentration.

C-XIV.5 15:20

ENABLING SOI INSPECTION FOR THE 65NM TECHNOLOGY NODE AND BEYOND

Wayne McMillan, Surfscan Division, KLA-Tencor, USA

SOI enables higher performance devices with lower power consumption. SOI adoption has started. Most IC customers are evaluating samples and some, such as IBM and AMD are running high volume production.

At the 65nm node, SOI and strained silicon substrate adoption will increase rapidly. Yield management for such design rules requires advanced defect inspection strategies. High-end logic device manufacturers desire SOI defect inspection specifications similar to Epi substrates.

Such sensitivity is not achievable on SOI with the inspection tools of today. This paper covers some of the fundamental physics that drives achievable sensitivity. A new inspection system that is able to deliver the required sensitivity is introduced. Sensitivity independent of SOI thickness and uniformity is demonstrated. The ability to use a single inspection recipe regardless of SOI thickness and uniformity is demonstrated.

A key inspection enabler of the era of SOI as a mainstream substrate for IC manufacturing is believed to be essential.

C-XIV.6 15:40

DESIGN, FABRICATION AND OPTICAL CHARACTERIZATION OF THIN 2-DIMENSIONAL Si_3N_4 WAVEGUIDES

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In view of the integration within Si-based optical devices, LPCVD (low pressure chemical vapor deposition) thin film Si_3N_4 waveguides have been fabricated on Si substrate within a CMOS fabrication pilot-line. Different structures (channel, rib and strip-loaded) were designed, fabricated and characterized both optically and structurally to optimize waveguide performances. Geometry, sidewall as well as layer roughness of the waveguides have been investigated by Scanning Electron Microscopy and Atomic Force Microscopy. Optical modes have been observed with a mode analyzer and compared with the results from simulation to confirm the process parameters. Propagation loss measurements at 780 nm have been performed by using both the cut-back technique and measuring the drop of intensity of the top scattered light along the length of the waveguide: best results have been obtained for channel waveguides, which have shown propagation losses of about 0.2 dB/cm. Differences between geometry and lithographic processes have been explained according to simulated results.

Optical guided modes have been measured also in the near-infrared range: preliminary results show propagation losses at 1310 and 1550 nm quite larger (about few dB/cm) than in the visible. This is due to the poorer confinement factor. To optimize confinement factor in the near-infrared, new waveguide designs and geometries (i.e. variable core gradient) were realized, and the data will be discussed at the conference.