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E-MRS Spring Meeting 2004
May 24-28, 2004

SYMPOSIUM B

Materials science issues in advanced CMOS source-drain engineering

Symposium Organizers:

Giovanni Mannino, CNR-IMM, Catania, Italy

Thomas Feudel, AMD Saxony LLC & Co. KG, Dresden, Germany

Peter Pichler, Fraunhofer IISB, Erlangen, Germany

Marco Servidori, CNR-IMM, Bologna, Italy

Papers will be published in **Materials Science and Engineering B**

E-MRS 2004 SPRING MEETING

SYMPOSIUM B

Tuesday, May 25, 2004 — Morning

08:50 **WELCOME G. Mannino** (CNR-IMM Catania, Italy)

Session I: Future trends in electronics
Session chair: G. Mannino (CNR-IMM Catania, Italy)

B-I.1 09:10 -Invited-

AMBIENT INTELLIGENCE : ENABLING PROCESS TECHNOLOGY
C. J. van der Poel, Philips Research Leuven, Belgium
As a result of the ongoing miniaturization of electronic circuits and the corresponding exponential increase in embedded computational power, we are reaching the point where it becomes viable to integrate electronics into people environments. Ambient Intelligence refers to an electronic environment that is sensitive and responsive to the presence of people. Such an environment should be
- ubiquitous: surrounding the user by a multitude of interconnected systems
- transparent: integrated and "hidden" into the background
- intelligent: adapting to the people that live in it
This paper makes an attempt at translating these high level needs into demands for Silicon process technology

B-I.2 09:50 -Invited-

SUB-50NM GATE LENGTH SOI TRANSISTOR DEVELOPMENT FOR HIGH PERFORMANCE MICROPROCESSORS
M. Horstmann, T. Feudel, A. Wei, M. Gerhardt, K. Frohberg, C. Schwan, M. Lenski, R. Stephan, K. Wieczorek, G. Burbach, A. Sultan, J. Cheek, D. Greenlaw and M. Raab; AMD Saxony LLC & Co. KG, Dresden, Germany
SOI technologies have reached maturity for production of high speed, low power microprocessors. This paper will high light several challenges found during the course of development for bringing 45nm LGATE SOI transistors into volume manufacturing. The key innovations developed for this transistor are a unique “Triple Spacer” structure, stressed liner films inducing strain in the channel, and highly optimised junctions. The novel “Triple Spacer” structure featuring individually controlled multiple offset spacers provides excellent DC characteristics and fine device tuneability for AC performance compared to conventional transistors. Channel strain induced by a stressed liner film increases mobility resulting in a significantly higher trans-conductance. Due to the use of tailored junctions, aggressive spike RTA as well as offset spacers, extremely low parasitic capacitances could be realized. The found improvements are highly manufacturable and result in an outstanding ring oscillator speed with an unloaded inverter delay of 6ps at reasonable leakage. Details of the device structure and the electrical performance as well as an outlook will be given at the conference.

10:30 **BREAK**

Session II: Advanced devices
Session chair: P. Pichler (IISB-FHG, Germany)

B-II.1 10:50 -Invited-

NEW PHYSICS MECHANISMS ENABLED BY ADVANCED SOI CMOS ENGINEERING
S. Cristoloveanu, IMEP (UMR CNRS, INPG & UJF), Grenoble, France
The limits of the conventional CMOS scaling become visible and generate renewed interest in SOI technology. However, in order to break the 10-nm MOSFET barrier, advanced concepts for transistor architecture are needed. The aim of this work is to analyze recent experiments and models. - SOI MOSFETs with ultra thin gate oxide, where gate-induced floating body effects occur. - SOI MOSFETs with ultra thin body (10 nm), showing quantum confinement, giant coupling effects between the two channels and thinning-related mobility degradation. - Double-gate MOSFETs with volume inversion; length-asymmetrical gates enable the reduction in source-drain series resistance by field effect. - SOI MOSFETs with three or four gates, where several channels and conduction mechanisms are simultaneously activated. - SOI MOSFETs with alternative buried dielectrics to limit self-heating and mobility degradation.

B-II.2 11:30

OPTIMIZATION AND UNDERSTANDING OF THRESHOLD VOLTAGE ROLL-OFF BEHAVIOR OF 65-nm TECHNOLOGY NODE nMOS AND pMOS BULK AND SOI MISFETs
A. Erlebach(a), A. Schenk(b), T. Feudel(c) and C. Zechner (a); (a) ISE AG, Zurich, Switzerland, (b) ETH Zurich, Switzerland, (c) AMD Saxony LLC and Co. KG, Dresden, Germany
In deep sub-um technologies, one of the main goals is the improvement of the threshold voltage (Vt) roll-off behavior. Using well-calibrated process and device simulation tools, we have studied the influence of the doping gradients of drain extension and HALO profiles on the Vt roll off behavior. In a first step, the process simulator has been calibrated by using SIMS profiles. During device simulation, critical transistor parameters like threshold voltage and overlap capacitance were kept constant at the nominal gate length by re-adjusting halo dose and offset spacer width. It was found that the influence of the drain extension doping gradient is small under these circumstances. On the other hand, the doping gradient of the HALO profile close to the

junction affects the roll-off behavior. Optimizing this gradient, it will be possible to improve the transistor performance without altering the nominal transistor parameters. Optimization of nmos and pmos HALO profiles with the respect to transistor parameters is done for a process with a gate length of 50 nm and below. A combination of process parameters is proposed that gives best transistor performance.

B-II.3 11:50

DAMAGE AND RECOVERY IN DOPED SOI LAYERS AFTER HIGH ENERGY IMPLANTATION

M. Ferri, S. Solmi, A. Armigliato, M. Bianconi, G. Lulli and D. Nobili; CNR-IMM Bologna, Italy

Silicon on insulator (SOI) substrates, uniformly doped n or p-type by ion implantation and annealing at different concentrations in the range 1-8x1020 cm-3, have been successively implanted with increasing doses of high energy (2 MeV) Si+ ions. The effects of irradiation, and the subsequent recovery have been followed by electrical conductivity and carrier mobility measurements. Isothermal annealings have been performed at temperatures in the range 550-800°C. The behavior of irradiated specimens has been compared with the one of reference undamaged samples of the same composition. The evolution of the irradiation damage and the recovery process have also been followed by Rutherford backscattering-channeling analysis, as well as by transmission electron microscopy observations. In As doped Silicon the irradiation induces a very high reduction of the carrier density, which saturates at a Si+ fluence of 5x1015 cm-2. Recovery takes place in two stages, at rates which increase with temperature and dopant concentration. The kinetics of these phenomena have been determined. Our results indicate that electron trapping is the responsible of the reduction of the carrier density upon irradiation; the nature and the thermal evolution of the structural defects is reported and discussed. A Similar work is in progress on Boron doped Silicon layers and the results will be reported.

B-II.4 12:30

FORMATION OF ULTRA-SHALLOW P+/N JUNCTIONS IN SILICON-ON-INSULATOR (SOI) SUBSTRATE USING LASER ANNEALING

K. K. Ong(a), K. L. Pey(a), P. S. Lee(b), K. L. Yeo (c), A. T. S. Wee, (c), Y. F. Chong(d) and X. C. Wang(e); (a) School of EEE, Nanyang Technology University, Singapore, (b) School of Materials Engineering, Nanyang Technological University, Singapore (c) Department of Physics, National University of Singapore, Singapore (d) Chartered Semiconductor Manufacturing Ltd, Singapore (e) Singapore Institute of Manufacturing Technology, Singapore

Laser annealing (LA), in which the laser melts the surface layer of silicon and causes the dopants to be distributed uniformly within the melted region, produces abrupt, highly activated and ultrashallow junctions. The degree of melting is determined by the extent of laser absorption and rate of heat dissipation, which is dependent of substrate properties. As the thermal conductivity of silicon dioxide is significantly lower than that of silicon, the silicon film on the buried oxide (BOX) layer is thermally insulated from the bottom substrate, depriving it of a good heat dissipation pathway. A lower laser fluence would be required to melt or/and activate the dopants in SOI. This work compares the redistribution of boron atoms in silicon (100) and SOI substrates after laser annealing. SIMS analysis shows that laser induced melting is significantly deeper for SOI than silicon substrates using the same laser fluence. The enhancement of melting is attributed to the heat insulating effect of the BOX layer. With multiple-pulse LA, the melt depth in SOI increases with subsequent laser pulses, a feature that is absent in silicon substrate. In SOI substrate, the sheet resistance remains relatively constant regardless of deeper junction formed with multiple pulse conditions, implying maximum dopant activation at given laser fluence is reached. Single- and multiple-pulse non-melt laser annealing of SOI are also explored. Boron profiles annealed in the non-melt region with 20 laser pulses or less overlaps with the as-implanted profiles, suggesting that no melting has occurred. However, significant melting is observed at 50-pulse annealing. The corresponding sheet resistance shows a sharp decrease with the initial pulses and consequently reaches a relatively constant level.

B-II.5 12:30

SOURCE-DRAIN ENGINEERING CHALLENGES IN FINFET DEVICE FABRICATION

D. Pham(a), H.-J. Li(b), B. Nguyen, G. Gebara, D. Larison, B. Sassman, B. Foran and L. Larson, International SEMATECH Austin TX U. S. A., (a) Motorola Assignee, (b) Infineon Assignee

Double-gate devices are considered most promising for scaling into the sub-20nm regime due to a steeper sub-threshold slope, reduced short channel effects, improved mobility, and drive current. The FINFET is one of the most attractive double-gate structure and most compatible with today's standard processing technologies. One of the challenging issues of fabricating FinFETs device is the doping of the source-drain junction in the Fin area. In planar device junction formation, the dopant is implanted onto a planar surface and can be monitored and analyzed by several standard techniques. These methods cannot be applied for FinFET junction formation due to the ultra-thin vertical dimension of the Fin. Implanting perpendicular to the wafer surface might not be the effective way to distribute the dopant uniformly across the Fin height due to the small surface area of the Fin. Also, due to silicon channeling, angle implantation might create dopant channeling through the ultra-thin Fin. Our simulation data illustrate the results of dopant distribution into a single Fin structure (35nm W x 55nm H) after several boron implantation conditions. The results demonstrate that a high angle of implantation at certain energy is needed to maximize the dopant distribution in the Fin. However, the maximum usable implant angle is limited by the packing density of the Fins. Further more, the amorphization in the fin area due to implantation might occur. As previously observed in FDSOI, amorphization of the thin silicon layer might suppress the regrowth due to lack of silicon crystal which might lead to higher resistivity and higher leakage. Several simulation data are verified with electrical resistivity measured on the Fin test structure and by the electron holography technique

12:50 **LUNCH**

Tuesday, May 25, 2004 Afternoon

Session III: Silicides I
Session chair: T. Metzger (ESRF, France)

B-III.1 14:10 -Invited-

NI-BASED SILICIDES FOR 45 NM CMOS AND BEYOND

A. Lauwers(a), J. A. Kittl(b), M. Van Dal(c), O. Chamirian(a), M. A. Pawlak(a), M. de Potter(a), R. Lindsay(a), X. Pages(d) and K. Maex(a); (a) IMEC, Leuven, Belgium, (b) Affiliate researcher at IMEC from Texas Instruments, (c) Philips Research Leuven, Belgium, (d) ASM Belgium, IMEC

Ni-silicide has been identified as the best candidate for 45 nm CMOS and beyond for several reasons : low formation temperature, low Si consumption, low contact resistance, low sheet resistance in narrow features and compatibility with ultra-shallow extension junctions. Ni-silicide is also compatible with SiGe substrates that are being introduced for mobility enhancement. In addition, NiSi is an attractive material for implementation as a metal gate. For the successful implementation of NiSi into CMOS flows, it is important to develop a full understanding of its key material issues and their impact on devices. The low temperature kinetics of Ni-silicide formation were studied. In the case of the Ni/Si reaction, with Ni being the main moving species throughout the reaction, Ni deposited on top of isolation (or spacers) surrounding small active areas or gates can diffuse and react to form a much thicker silicide film on the small features. Excessive silicidation of small features can be prevented by a 2 step Ni-silicidation process with careful control of the thermal budget before the selective etch of the unreacted Ni. Conduction based RTP, allowing for high ramp rates and spike anneals, was compared to conventional lamp based RTP. Understanding of the reaction kinetics is also important for the implementation of NiSi in fully silicided poly-Si gates. Major concern for implementation of NiSi is its poor thermal stability. The use of alloying elements such as Pt and Ta to improve the thermal stability was studied. The thermal stability of Ni-silicide on SiGe substrates was investigated. Another key issue is the formation already at low temperature of pyramidal NiSi2 grains, which are detrimental for interface roughness.

B-III.2 14:50

THIN NICKEL SILICIDE LAYER FORMATION ON SILICON ON INSULATOR (SOI) MATERIAL

A. Alberti(a), B. Cafra(a), G. Mannino(a), M. Servidori(b), T. Kammler(c) and T. Feudel(c); (a) CNR-IMM Catania, Italy, (b) CNR-IMM Bologna, Italy, (c) AMD Saxony LLC & Co. KG, Dresden, Germany

Nickel monosilicide thin layers (NiSi) are planned to be used on the next generation metal-oxide-semiconductor devices (MOSFET) to replace cobalt disilicides as metallization of gates and diffusion areas. The main advantage of using NiSi instead of CoSi2 consists of reducing silicon consumption without increasing sheet resistance to assure the shallow junction integrity and a low contact resistance. Nevertheless, NiSi thin layers tend to be converted into the more resistive NiSi2 phase as the thermal budget exceeds 700-800°C. In this work we have studied the phase transition of a 7 nm thin Ni layer grown on standard silicon and SOI (Silicon on Insulator) wafers implanted with As at different doses. We have investigated thermal stability of the NiSi phase using fast ramp rates and spike thermal processes which are widely used to preserve shallow junction from dopant diffusion during electrical activation. Nickel reaction has been performed in nitrogen ambient in the temperature range from 450 to 1125°C and has been studied by sheet resistance measurements, TEM and XRD analyses. It has been found that, in spite of the thin layer used, spike annealing processes allow the stability window to be extended above 900°C preserving the NiSi layer from structural degradation. Moreover, the range of stability is significantly affected by the As dose used and by the presence of the buried oxide layer in the SOI wafers.

B-III.3 15:10

THE STUDY OF THERMAL STABILITY OF Ni(Si1-xGex) FILM WITH THE Ge CONTENTS

J.-S. Kim(a), D. Lee(a), K. Do(a), D.-H. Ko(a), J.-H. Ku(b), S. Choi(b) and C.-W. Yang(c); (a) Yonsei Univ. Dept. of Ceramic Engineering, Seoul, Korea, (b) Process Development Team, Semiconductor R&D Division, Samsung Electronics Ltd. Korea, (c) Sungkyunkwan Univ. School of Metallurgical and Materials Engineering, Suwon, Korea

SiGe CMOS devices have the potentials for future applications in ULSI circuit technology. As gate material, it is effective to reduce Boron penetration and gate depletion. It is also known that the SiGe substrate in the source/drain and channel region is able to obtain shallow junction and high carrier mobility. On the other hand, for high performance device, Ni SALicide process is good candidate due to small contact resistance, low silicon consumption, no bridging failure property and no line width dependence. However, as post-annealing, the increase of sheet resistance occurs for NiSi2 formation and segregation. In this study, we investigated the formation of Ni(Si1-xGex) films with Ge contents. First, ~30nm Ni films are deposited on epi-Si1-xGex(x=0, 0.1, 0.2) substrate by DC magnetron sputtering. And Ni(Si1-xGex) films were formed by RTP in N2 ambient. The thickness and composition of Ni(Si1-xGex) films were confirmed by RBS. In order to analyze the electrical property, phase identification and microstructure, Rs and XRD measurement were used. In the Ni/Si system, NiSi was formed until 700°C, and segregated at 900°C. However, the segregation temperature decrease upon Ge contents in the Ni/SiGe system. And in order to observe the thermal stability of Ni(Si1-xGex) upon Ge contents, the silicide samples annealed at 540°C is post-treated in furnace at 600, 650°C for 210, 60 minutes. As the results, the sheet resistance of Ni/SiGe system increased more sharply than one of Ni/Si system.

B-III.4 15:30

NICKEL SILICIDES IN SEMICONDUCTOR PROCESSING: THERMAL BUDGET CONSIDERATIONS

S. Ramamurthy(a), B. Ramachandran(a), A. Hunter(a), R. Thompson(b) and C. B. Carter(b); (a) Front End Products Group, Applied Materials Inc., Sunnyvale CA, U. S. A., (b) Department of Chemical Engineering & Materials Science, University of Minnesota, Minneapolis MN, U. S. A.

Although Nickel Silicide offers numerous benefits over Cobalt and Titanium silicides for contact metallization in the silicon devices, integration issues need to be addressed. These issues may be related to surface preparation, substrate condition (doped-, poly-, SiGe), metal layer deposition conditions (temperature,

cap layer) and thermal anneal scheme (1-step vs. 2-step RTP). Conventional RTP technology faces challenges with the measurement and control of wafer temperatures in the sub-300C regime. Modifications have been made to the processing environment including measurement technology to facilitate sub-300C processing. In this work, sheet resistance and microscopy characterization methodologies have been used to correlate film properties to varying thermal exposures in the temperature range from below 300C up to 600C. Transmission electron microscopy has been used to study the interfaces between the different phases to comprehend the reaction mechanisms of various thermal budgets. Since a vast number of integration factors affect the ultimate resistivity of the desired silicide phase, it is vital to establish a temperature monitoring methodology to delineate the effects of thermal exposure from other factors. Quantitative low temperature control data and advances made in lamp-based RTP technology will be discussed in this paper.

15:50 **BREAK**

16:10 **POSTER SESSION I**

B/PI.01 AUGER AND XPS CHARACTERIZATION OF A MULTI LAYERED Ti-Co-Si SYSTEM FOR SELF ALIGNED SILICIDES PURPOSES: A STOICHIOMETRY AND CHEMICAL INVESTIGATION

S. G. Alberici, A. Giussani and E. Ravizza, STMicroelectronics, Physics and Material Characterization Lab., Central R&D Division, Agrate Brianza, Italy

Self-Aligned Silicides, as the Co-Si system, for less than 0.13 µm applications, are still under investigation, due to some lack of their structural and basic property knowledge. Due to Oxygen contamination once exposed to air, an outermost capping layer is required to ensure that no Oxygen can enter the network, altering the Thermodynamic properties of the film itself, when performing any thermal treatment. With this in mind, in the following work we present an Auger Electron Spectroscopy (AES) and an X-ray Photoelectron Spectroscopy (XPS) investigation on a Ti-Co-Si multi layered stacked system, thermally treated in the range 1023 - 1103 K, to look at the apparent Stoichiometry (by AES) and to the chemical role of Ti (by XPS) after making such an annealing procedure. It turns out that the CoSi2 phase is formed after annealing at 1023 K, and that the Ti cap layer has functioned as a strong Oxygen barrier diffusion at this temperature range, forming a TiO2 oxide right at the top of the multi layer, which is the Ti oxide compound foreseen by Thermodynamics at these conditions. Part of the remaining Ti could be still present into the Co-Si matrix, likely having formed a ternary compound that can be responsible for a different reaction Kinetics too.

B/PI.02 STUDY OF THE COSI2 DEFECTS INDUCED BY 300MM SOFT SPUTTER ETCH PROCESS BEFORE COBALT DEPOSITION

A. Humbert(a), C. Regnier(b) and G. Braeckelmann(c); (a) Crolles2 Alliance –Philips, (b) Crolles2 Alliance –ST Microelectronics, (c) Crolles2 Alliance –Motorola, Crolles, France

A critical step in the cobalt silicide formation is the Soft Sputter Etch (SSE) before Co deposition. [1]. It has to remove native oxide and impurities to ensure a clean surface, but it should also be soft enough to avoid leakages and resputtering. In this paper, the 300mm SSE chamber behavior is analyzed on blanket and 90nm patterned wafers to explain the formation mechanism of defects observed in salicided areas. Defectivity has been observed along the spacers, especially in pinched active structures. A nitrogen analysis performed by μ-Auger showed that nitride from the spacers was re-sputtered on the active areas during the SSE process, subsequently blocking the salicidation. DOE on blanket wafers were run characterizing the 300mm chamber behavior. No major differences were seen between 200 and 300mm chambers on blanket wafers. Etch rate was found to be mainly dependent on the RF bias power , whereas both RF bias and RF coil powers influenced the DC bias voltage on the wafer during process. Furthermore, a DOE on 90nm patterned wafers was performed in order to reduce nitride resputtering and thereby improve defectivity and device performance. Results showed that optimizing the ratio between RF bias and RF coil and changing both RF values was a way to improve the salicidation process. [1] Abu H.M Kamal, Nicholas S. Argenti, and Chris S. Blair, IEEE transaction on semiconductor manufacturing, Vol15, N°3, august 2002.

B/PI.03 THE EFFECT OF THE RAPID THERMAL ANNEALING ON THE INTERDIFFUSION AND THE REACTION AT THE INTERFACE OF THE BINARY SYSTEME Cr/Si

A. Merabet and R. Mezouar, Laboratoire Physique et Mécanique des Matériaux Métalliques, Faculté des Sciences de l'Ingénieur, Université de Sétif, Algérie

The silicides of the refratary metals are, in general, used to shunt either the Si-poly at the level of the grille in order to lower its resistivity or the source and drain regions by a silicide metalisation self-aligned in these zones. In order to understand the growth mecanism of the silicides and the effect of the dopant on the electrical activity, a thin layer of chrome (1000 Å) is deposited via electronic bombardment on the silicon (100) substrate implanted and non implanted at the arsenic at 100 KeV with a dose of 1015 at.cm-2. Afterwards, we perform a rapid thermal annealing in the interval of temperature [450-600°C] and for a duration of 15 to 60 secondes, in order to permit the formation of silicides and the electrical activity of ions. The analysis of the samples by XRD and RBS showed that the rapid thermal annealing leads to a reaction at the interface Cr/Si inducing the formation and the growth of the unique silicide CrSi2. It is also established that the kenematic growth of CrSi2 presents a linear evolution with temperature and time. This fact shows that the growth is governed by a chemical reaction of the interface. The variation of the sheet resistance in fonction of the time and temperature increases suddenly at the begining and then stabilises at about 125 and 180 Ω/ڤ for Cr/Si and Cr/Si (As) respectively. This shows that the electrical activity is satured above 500 °C. The presence of the implanted arsenic in the single crystal silicon incraesed the resistance in a significatif manner. This fact permits us to conclude that after silicidation, the atoms of the dopant diffuse the silicium in the layer of the silicide of chrome and accumulate at the surface, which induces an increase of the resistance.

B/PI.04 ELECTRICAL CHARACTERIZATION OF TiSi/Si-Ge-C SCHOTTKY DIODES

A. R. Saha(a), S. Chattopadhyay(b) and C. K. Maiti(a); (a) Department of Electronics & ECE, IIT Kharagpur, India, (b) School of Electrical, Electronics and Computer Eng., Univ. of New Castle upon Tyne, U. K.

The incorporation of carbon on the Si/SiGe material system,open a new era in band gap engineering of Si based heterostructure devices.As the Si-Ge-C alloy structures permit a band offset in the valence and conduction band, both hole and electron confinements are possible.Hence carbon incorporation into SiGe alloys has attracted much attention in the fabrication of hetero-bipolar devices.In this work, we have studied Ti-silicided Schottky as a possible metallic contact on Si-Ge-C alloy layer, in terms of its electrical characteristics and stability.The partially strain compensated Si-Ge-C samples, used in our study, have 20% Ge and 1% C concentration in the epi-layer. One set of sample has a Si cap layer of 50Å thickness. From the current voltage characteristics, it has been observed that the reverse current across the Schottky diode (without Si cap layer) is higher than that across the diode with a Si cap layer, although they have the same Ge and C concentrations. This is attributed to the inhomogeneous and nonuniform interface during silicidation. In the absence of a Si cap layer, metal reacts directly with Si-Ge-C films resulting in a nonuniform interface.The variation of the ideality factor and barrier heights with temperature is found to be similar for all the diodes.The values of ideality factors for TiSi/Si-Ge-C diodes are in the range of 1.1–1.7.The result shows that a high non-ideality at the interface for the Si-Ge-C Schottky diode without a Si cap layer. The results are also compared with a similar TiSi/Si Schottky diode processed in the same run.

B/PI.05 THERMAL STABILITY OF NICKEL GERMANOSILICIDE ON ION-IMPLANTED SI0.8GE0.2

T.-H. Yang(a), E. Y. Chang(a), S.-L. Hsu(b), T.-Y. Yang(c), G.-L. Luo(d), H.-C. Tseng(e) and C.-Y. Chang(a); (a) Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan, R. O. C., (b) National Nano Device

Laboratories, Hsinchu, Taiwan, R. O. C., (c) Department of Materials Engineering, Tatung University, Taipei, Taiwan, R. O. C., (d) Microelectronics and Information Systems Research Center, Hsinchu, Taiwan, R. O. C., (e) United Microelectronics Corporation, Hsinchu, Taiwan, R. O. C.

Thermal stability of the nickel germanosilicide formed on the high and low-dose B, BF2, P and As -implanted Si0.8Ge0.2 epilayers was investigated by scanning electron microscopy (SEM) and transmission electron microscopy (TEM) as well as by sheet resistance measurement. It was found that the thermal stability of the nickel germanosilicide formed was significantly affected by the implantation species in the Si0.8Ge0.2 epilayers and BF2 is superior than other species used in this study. In high and low-dose B, P and As-implanted samples, agglomeration of nickel germanosilicide became very severe after rapid thermal annealing (RTA) at 800℃ for 30s. In high and low-dose BF2-implanted samples, there was less nickel germanosilicide agglomeration as compared to the Si0.8Ge0.2 implanted by other chemical species. Comparing the samples with high and low-dose BF2-implantion, it was found that the sheet resistance of the high-dose sample was lower than that of the low-dose samples and the density of the agglomeration was lower in the high-dose-implanted sample. The results are attributed to the retardation of the formation of the agglomerates due to the presence of fluorine dose in the nickel germanosilicide layers.

B/PI.06 TUNGSTEN SILICIDE CONTACTS TO POLYCRYSTALLINE SILICON AND SILICON-GERMANIUM ALLOYS

G. Srinivasan, M. F. Bain, S. Bhattacharyya, P. Baine, B. M. Armstrong, H. S. Gamble and D. W. McNeill, Northern Ireland Semiconductor Research Centre, Queen’s University, School of Electrical and Electronic Engineering, Belfast, U. K.

Modern MOS transistors employ novel device architecture. A key issue is source-drain engineering of MOSFETs which requires critical control over the junction depth. Raised source/drain (or recess-gate) MOSFETs offer advantages in decreasing junction depth resulting in reduction in punch-through and SCE problems. Polycrystalline silicon or silicon-germanium can be deposited for the raised source/drain. SiGe is preferred due to its lower resistance. While this lowers series resistance, the contact resistance of metal or metal silicides to the source/drain remains a serious issue at sub-micron dimensions and must be minimised. In this work, WSi2 has been investigated as a contact metallization to boron doped polycrystalline Si1-xGex, with 0 ≤ x ≤ 0.3. Cross Bridge Kelvin Resistor structures were fabricated incorporating CVD WSi2 and SiGe. A very significant reduction has been measured in specific contact resistance from 4 x 10-7 to 5 x 10-8 ohm.cm2 as x is varied from 0 to 0.3. The reduction in specific contact resistance is attributed to energy band modification due to the inclusion of germanium in the layer, and also due to greater activation of dopant in the polycrystalline Si1-xGex compared to polysilicon. This paper will outline the technology and results in detail. Issues of silicide structure, grain size and out-diffusion of source drain dopants will also be addressed.

B/PI.07 THERMAL STABILITY OF NICKEL SILICIDE ON SILICON ON INSULATOR (SOI) MATERIAL

B. Cafra(a), A. Alberti(a), L. Ottaviano(a), C. Bongiorno(a), G. Mannino(a), T. Kammler(b) and T. Feudel(b); (b) CNR-IMM Catania, Italy, (b) AMD Saxony LLC & Co. KG, Dresden, Germany

Metal silicide thin films grown on silicon wafers play an important role on ultra scaled MOS transistors mainly because they affect diffusion and contact resistances. Device shrinking causes the increasing of contact resistance and hence involves scaling of silicide layer thickness to reduce silicon consumption during the salicide process. Nowadays, new materials like Ni silicide and ternary compound are considered suitable for the salicidation process. This paper presents a study on the thermal stability of NiSi silicide in the temperature range between 450 and 1125°C, grown on two different substrates: standard silicon and SOI substrate, both doped with As atoms at a dose of 21015/cm2. Silicidation has been performed by means of spike annealing processes and has been studied by sheet resitance, TEM and XRD analyses. Ni monosilicide was found to be the stable phase in the temperature range from 600 to 900°C. At lower temperatures Ni2Si coexists with NiSi phase. At temperatures higher than 900°C NiSi starts to be converted into NiSi2. NiSi transformation after 900°C, NiSi2 agglomeration phenomena and the presence of unconnected NiSi2 silicide grains are strictly related to the observed increase in sheet resistance. It has also been found that the substrate on which Ni atoms have been deposited plays an important role, particularly preventing the formation of silicide “island” at higher temperatures when SOI wafers are used.

B/PI.08 TIME RESOLVED COSI2 REACTION IN PRESENCE OF TI AND TIN CAP LAYERS

A. Alberti(a), R. Fronterré(a,b), F. La Via (a) and E. Rimini(b); (a) CNR-IMM Catania, Italy, (b) Dipartimento di Fisica e Astronomia dell’Università di Catania, Italy

CoSi2 thin layers on polycrystalline silicon are nowadays used in place of TiSi2 as gate metallization of MOS devices. Due to the need of using Ti or TiN layers as a barrier against contaminant species diffusing in silicon, it is required to cover cobalt by these cap layers before silicide reaction. In this work we have compared the reaction of a reference Co/Si sample to the cases of a Co layer capped with Ti or TiN thin films. In order to study how these systems evolve toward the stable CoSi2 phase, we have performed time resolved sheet resistance measurements during isothermal annealing in the temperature range between 400 and 500°C in a vacuum chamber. The resistance curves are characterised by a transition peak whose properties depend on the cap layer type and the annealing temperature. The critical stages of the transformation and the characteristic time intervals have been extracted and studied in detail. We have found that the TiN layer does not remarkably affect Co phase transition whilst Ti systematically introduces a delay time needed to complete Co2Si, CoSi and CoSi2 reactions. This effect is finally responsible for electrical and structural changes with respect to the reference case.

B/PI.09 STRUCTURAL CHARACTERISATION OF NICKEL SILICIDE PERFORMED BY TWO-DIMENSIONAL X-RAY MICRODIFFRACTION

P. Colombi(a), E. Bontempi(a), U. M. Meotto(b), S. Porro(b), G. Richieri(c), L. Merlin(c) and L. E. Depero(a); (a) INSTM and Dipartimento di Ingegneria Meccanica, Università di Brescia, Italy, (b) INFM-Dipartimento di Fisica, Politecnico di Torino, Italy, (c) IRCI-International Rectifier Corporation Italia, Borgaro Torinese, Italy

Silicon carbide is a wide band gap semiconductor very attractive for applications in high power, high frequency and high temperature electronic devices. Even if its properties are very promising, the realization of SiC based devices presents several problems. In this work we have studied the interface between SiC and the metal with the aim of ohmic contact optimisation. In particular the ohmic contact formation mechanism for the systems Ni/4H-SiC have been considered and discussed. Several synterization conditions in the range of temperatures between 300°C and 1050°C have been performed in order to understand the chemical reactions at the interface. The thermal processes have been conducted in a hot furnace in controlled atmosphere with cooling ramp of 40°/min. The formation of graphite on the surface and metal silicides at the interface have been followed by using micro x-ray diffraction and micro Raman techniques. The combined analysis of the two measurements allowed the recognition of all the formed phases at the interfaces. In particular, micro x-ray diffraction technique offered the advantage to study the preferred orientation and the stress in the silicide phases in a easy and fast way.

B/PI.10 CHARACTERIZATION OF PTSI SILICIDE FOR A SOI SELF ALIGNED MOSFET NANO-TRANSISTOR

M. Derras(a,b) and A. Kadoun(b); (a) Faculté d'Electronique et d'Informatique - USTHB, Alger, Algeria, (b) Université Djillali Liabès de Sidi Bel Abbès, Algeria

Very thin films of metal silicides play an increasing important role in silicon integrated circuit technology as MOSFETs are shrunk below 0.1 mm of gate length. In order to further pursue down-scaling of MOSFETs in the 10-20 nm range of gate lengths, a significant effort must be devoted to the development of a new architectures based on the low resistivity, and reduced silicide/silicon specific contact resistance. Pt based silicides is probably the best candidates for that purpose. In this paper, we propose, first provides a detailed analysis of the formation of Pt2Si and PtSi silicides, based on XPS, TEM and electrical characterizations. Published kinetics of the Pt2Si and PtSi transformations under UHV condition are consolidated on the basis of XPS measurements performed during an in situ annealing at a constant heating rate. Using rapid thermal annealing at 300, 400 and 500°C, the sequential Pt-Pt2Si-PtSi reaction chain is found to be completed within 2 minutes. Pile up of oxygen occurring at the Pt2Si/Pt reaction front is clearly identified as an inhibiting factor of the silicidation mechanism. Another incomplete reaction scheme limited to the unique formation of Pt2Si is exemplified in the case of ultra thin SOI films. Finally, current drive measurements on PtSi Schottky contacts have allowed to identify 300°C as the optimum annealing temperature while TEM cross-sections demonstrates the formation of a smooth and continuous PtSi/Si interface at 300°C.

B/PI.11 THE STUDY OF MICROSTRUCTURE OF NiSi FORMED BY Ni1-xTax(x=0.05, 0.1, 0.15 and 0.2) ALLOY

D. Lee(a), K. Do(a), D.-H. Ko(a), S. Choi(b), J.-H. Ku(b) and C.-W. Yang(c); (a) Yonsei Univ., Dept. of Ceramic Engineering, Seoul, Korea, (b) Process Development Team, Semiconductor R&D Division, Samsung Electronics Ltd. Korea, (c) Sungkyunkwan Univ. School of Metallurgical and Materials Engineering, Suwon, Korea

For high performance device, Ni SALicide process is good candidate due to low contact resistance, low silicon consumption, no bridging failure and no line width dependence. However, there is demerit that the sheet resistance increasing of Ni silicide occurs for NiSi2 formation and segregation as post-annealing. In this paper, the comparative study of the silicide formation with Ni film and Ni1-xTax(x=0.05, 0.1, 0.15 and 0.2) alloy films deposited on the single crystal Si(100) substrate has been performed with various temperature. In the Ni/Si system, it was formed the NiSi until 700℃, and segregated at 900℃. However, the segregation temperature is up as Ta contents in the Ni-Ta alloy/Si system increase. And the sheet resistance of Ni silicide by Ni-Ta alloy/Si system has low values than one of Ni silicide by pure Ni/Si system in high RTP temperature range. It is expected that Ta (or Ta compounds) functions of the diffusion barrier in the grain boundary, and the phase transformation NiSi to NiSi2 are slow. After first annealing by RTP at 500℃, post anneal were performed at the different temperature, considering post thermal budget after salicide process. In case of Ni0.85Ta0.15/Si and Ni0.8Ta0.2/Si system, the Ni silicide layer has a stable sheet resistance of about 5Ω/sq. and maintained for 210 min long time annealing by vertical furnace at 600℃ and 650℃, but, the sheet resistance increase with increasing of annealing time due to formation of NiSi2 in Ni/Si system. The thickness and composition of Ni-Ta films were confirmed by RBS. Moreover, we analyzed the microstructure by using TEM and phase transition by XRD. These results show the improvement in the thermal and morphological stability of NiSi in case of Ni1-xTax/Si systems.

B/PI.12 EFFECT OF P+ IONS ON THE MICROSTRUCTURE AND THE NATURE OF THE FORMED SILICIDE IN THE Cr/Si SYSTEM

K. Mirouh(a), A. Bouabellou(a), R. Halimi(a), A. Karaali(a), A. Mosser(b) and G. Ehret(b); (a) Département de Physique Laboratoire des Couches Minces et Interfaces, Campus Chaab Errassas, Université Mentouri de Constantine, Algeria, (b) IPCMS-GSI, Strasbourg, France

The effect of the P+ ions on the microstructure and the formed silicide in the annealed Cr/Si system is studied. The chromium layer is deposited by electron gun evaporation on the undoped and P+ doped moncrystalline silicon. Cross-sectional transmission electron microscopy investigation of the samples annealed at 475°C for different times shows that the presence of phosphorus leads to the formation of CrSi2 disilicide free of defects and the Cr3Si silicide for lower and higher annealing times respectively. In the case of undoped substrate, the formed disilicide CrSi2 is stable and contains a high concentation of defects when the chromium is partially consumed.

B/PI.13 GRAIN SIZE AND ORIENTATION IN TERNARY Co(1-x)Ni(x)Si2 THIN FILMS ON Si(100): INFLUENCE OF THE Ni CONTENT

D. Smeets(a), C. Drijbooms(b), H. Bender(b) and A. Vantomme(a); (a) Instituut voor Kern- en stralingsfyscia, KU Leuven, Belgium, (b) IMEC, Leuven, Belgium

Thin (12nm) Co1-xNix (x = 0.05, 0.10, 0.25 and 0.50) films are e-gun co-evaporated at room temperature onto Si(100) in a UHV-system. In situ Auger electron spectroscopy (AES) proved that the Si-substrates were atomically clean after HF-treatment and a Si-beam clean procedure, prior to metal deposition. The disilicide is formed in a two-step rapid thermal process (RTP) in N2-ambient (RTP1; 540°C 1', RTP2; 600°C, 700°C, 800°C 1'). Rutherford backscattering and channelling spectrometry (RBS/C) shows an improved channelling effect with increasing Ni content, indicating an evolution from a polycrystalline CoSi2 film to a strongly textured Co0.50Ni0.50Si2 film. Detailed texture analysis is performed by X-ray diffraction (XRD). q-2q measurements and (220) XRD pole figures clearly show the presence of (111), (220), (311) and (211) oriented grains. With increasing Ni content the (111), (311) and (211) diffraction peaks become less intense and eventually disappear. While grains with these orientations vanish, the (220) oriented grains become the most prevailing (10% Ni). With further increasing Ni content the (220) oriented grains are gradually disappearing in favour of (100) oriented grains as evidenced by offset-scans. For a Ni content of 50% the (100) orientation is clearly the most prominent. The results are explained by phase separation occurring during monosilicide formation. AES sputter experiments show that a Ni rich (mono)silicide is first formed near the interface, thus promoting the formation of a Ni rich disilicide seed layer. With increasing Ni content the thicker seed layer will result in an increased tendency of the grains to preferentially grow along the (100) direction as is the case for a pure Ni layer.

B/PI.14 INDIUM DIFFUSION PROFILES IN THIN SIMOX SILICON-ON-INSULATOR

P. Chen(a), Z. H. An(b), M. Zhu(a,b), R. K. Y. Fu(a) and P. K. Chu(a); (a) Department of Physics and Materials Science, City University of Hong Kong, China, (b) Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China

The indium diffusion behavior and implant damage in separation by implantation of oxygen (SIMOX) substrate with 200nm top silicon layer at different implantation energies and doses were studied. Rutherford backscattering spectrometry in the channeling mode (RBS/C) and cross-sectional transmission electron microscope (X-TEM) were used to characterize the

implant damage before and after annealing. Secondary ion mass spectrometry (SIMS) was used to study the indium diffusion behavior in both the top Si layer and buried oxide layer of SIMOX. Our data indicate that the intrinsic defects in the top layer of SIMOX SOI have no obvious effects on indium diffusion and at low energy and low dose implantation, the indium diffusion profiles exhibit no significant differences compared with those in bulk silicon substrates. However, at a higher implantation energy and dose such as 200 keV and 11014 cm-2, the buried interface of SOI, which acts as a recombination center of point defects, can greatly affect the indium diffusion profile by trapping indium atoms in the top Si layer thus resulting in a very steep indium channel profile in the top silicon layer. Therefore, for high dose implantation, transient enhanced diffusion (TED) of indium has been observed to be less serious in SIMOX substrates than in bulk Si.

B/PI.15

STUDIES ON Al2O3-ZrO2 HIGH K GATE DIELECTRICS ON SILICON-ON-INSULATOR

C. Lin(a), M. Zhu(a,b), W. Liu (a) and P. K. Chu (b); (a) Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, China, (b) Department of Physics and Materials Science, City University of Hong Kong, China

Al2O3-ZrO2 composite films were prepared on silicon-on-insulator (SOI) substrate by ultra-high vacuum electron-beam co-evaporation and the as-deposited and annealed films were investigated. The amorphous and mixed structure is maintained up to an annealing temperature of 900˚C, which is much higher than that of pure ZrO2 film. Moreover, the expansion of the interfacial oxide layer and formation of silicide at high temperature are suppressed, indicating that the structure in the ZrO2-Al2O3 film is stable up to 900˚C. Our results also indicate a portion of the Al2O3-ZrO2 film becomes polycrystalline after 1000˚C annealing, and interfacial broadening is observed. Possible explanations are given to explain our observations.

B/PI.16

SiGe-ON-INSULATOR MATERIAL FABRICATION BY OXYGEN IMPLANTATION INTO SiGe/Si HETEROSTRUCTURE AND NOVEL TWO-STEP ANNEALING

M. Zhang(a), Z. An(a), C. Lin(a) and P. K. Chu(b); (a) The Research Center of Semiconductor Functional Film Engineering Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China, (b) Department of Physics and Material Science, City University of Hong Kong, China

Relaxed SiGe-on-insulator (SGOI) is a suitable material to fabricate strained Si structures. Separation-by-implantation-of-oxygen (SIMOX) is a competing method to synthesize SGOI materials. In this work, SiGe/Si samples were implanted with 3E17 cm-2 oxygen ions at 60 kV followed by a high temperature annealing process. Oxygen segregation and Ge diffusion during the annealing process were investigated using Rutherford backscattering spectroscopy/channeling, high-resolution x-ray diffraction, and high-resolution transmission electron microscopy. Our results show that the sample structure strongly depends on the thermal history and Ge diffuses mainly at the beginning stage of the high temperature process. The process can be improved by introducing an annealing step at a medium temperature before high temperature annealing and sharper interfaces and good crystal quality can be obtained. Our results indicate that our modified SIMOX process can fabricat high quality SGOI structure.

B/PI.17

ELECTRICAL ACTIVATION OF B AND AS IMPLANTS IN SILICON ON INSULATOR (SOI) WAFERS

L. Ottaviano(a), G. Mannino(a), V. Privitera(a), M. Herden(b) and T. Feudel(b); (a) CNR-IMM Catania, Italy, (b)AMD Saxony LLC & Co. KG, Dresden, Germany

It is well known that MOS devices fabricated on SOI substrates show several advantages with respect to those realised on silicon bulk. Here, we have investigated the mechanisms of atomic transport and electrical activation of dopants in very thin (100nm or 60nm) SOI materials manufactured with the Smart CutTM process. The samples have been doped with As or B, either implanted as B itself or through BF2, and then spike annealed in the temperature range 450-1125°C. For comparison, selected samples have been pre-amorphised. TEM, SIMS, SRP and sheet resistance measurements have been used as characterisation techniques. The sheet resistance measurements show that the RS values of SOI substrates implanted with As are higher than those of bulk Si for $T < 900$°C. In the case of BF2, the RS values measured in SOI samples are higher than that in bulk Si regardless of the temperature. SRP profiles of As show that for a 1000°C spike annealing treatment less diffusion is observed in SOI than in bulk Si, while at 1125°C the situation is inverted. It is argued that defects are trapped at the interface Si/SiO2 (1000°C, spike) and they are successively released (1125°C, spike). Both for bulk Si and for SOI, the carrier profiles measured in pre-amorphised samples are shallower, but less active, than those relative to samples without pre-amorphisation. Also in the case of implanted B samples we noted in the electrical profiles similar differences between Si bulk and SOI, where the pre-amorphization implant plays an important role.

B/PI.18

INVESTIGATION OF LOCAL STRESS FIELDS IN SI LINES ON SOI SUBSTRATE: FINITE ELEMENT MODELLING AND HIGH RESOLUTION X-RAY DIFFRACTION

A. Loubens(a,b), B. Charlet(c), O. Thomas(a) and R. Fortunier(b); (a) TECSEN UMR CNRS 6122, (b) Ecole Nationale Supérieure des Mines de Saint Etienne, centre SMS, (c) CEA LETI, France

The influence of local stress fields on the electrical properties of Si-based nanostructures is of increasing concern. The experimental evaluation of stresses at the required scale (few nanometres) remains, however, a very challenging task. We propose a non destructive X ray diffraction technique for local strain measurement using either laboratory or synchrotron radiation source .We analyzed an array of single crystal Si lines etched in SOI (Silicon On Insulator) substrate and capped by SiO2 and Si3 N4 stack. Reciprocal space maps were performed on the Si lattice from the lines which is rotated by some 45° from the base Silicon substrate lattice. X ray diffraction rocking curve performed on Si 004 and Si 224 reveal distinct superlattice peaks whose spacing is related to the in-plane periodicity. The intensity of these peaks is related to the local strain field. Reciprocal space maps obtained by High resolution diffraction are compared with maps calculated from displacement fields derived from finite element modelling. We will compare experimental and simulated intensities and conclude about the validity of FEM simulations as well as on this technique as an alternative route to micro diffraction experiments.

B/PI.19

SIMULATION OF SUPPRESSION OF FLOATING-BODY EFFECT IN PARTIALLY-DEPLETED SOI MOSFET USING A Si(1-x)Ge(x) SOURCE STRUCTURE

M. Zhu(a,b), P. Chen(a), R. K. Y. Fu(a), W. Liu(b), C. Lin(b) and P. K. Chu(a); (a) Department of Physics and Materials Science, City University of Hong Kong, China, (b) State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystems and Information Technology, Chinese Academy of Sciences, China

SOI devices are attracting attention as promising structures for low power as well as high performance ULSI devices. However, the biggest concern is the floating-body effect, which may impact the performance of SOI devices and circuits. We report the use of Si(1-x)Ge(x) source to suppress the floating-body effect in a partially depleted SOI MOSFET. Our work is

conducted using a two-dimensional device simulation program Medici. In the simulation, the relevant geometrical and technological parameters of the SOI MOSFET are as follows. The device has a 2E16 cm-3 p-type substrate with n-type source and drain doping of 2E18 cm-3. The channel length is 0.5μm, and the thicknesses of the gate oxide, top silicon and buried oxide are 10nm, 400nm and 400nm, respectively. Si1-xGex (x=0.2 and 0.4) layer is formed in the source region using Ge-implantation. The simulated band diagram indicates that Ge implantation leads to bandgap narrowing at the source, which may increase the hole absorption efficiency of the SiGe source. This should lead to an increase of the hole current in the narrow bandgap region as confirmed by the simulated hole current vectors diagram. In fact, dispersing the accumulated holes in the floating body is key to the suppression of the floating-body effect. Hence, the floating-body effect will be eliminated. The output characteristics, breakdown voltage, and threshold voltage of the source structure SOI MOSFET are simulated and compared with those of a conventional SOI device. As expected when using a new structure, the kink effect is reduced and the breakdown voltage is substantially increased. The effect of the suppression of the floating-body effect using a Si(0.6)Ge(0.4) source is more obvious than that of using a Si(0.8)Ge(0.2).

B/PI.20 A NEW MODEL OF THE EFFECTIVE MOBILITY IN MOS TRANSISTORS OPERATED FROM HELIUM TO ROOM TEMPERATURE

R. Rmaily and K. Rais, Université Chouaib Doukkali, Morroco

A New model of the effective mobility in MOS Transistors is proposed, it explain the negative transconductance in ohmic regime at high field, evaluated the surface roughness thickness, the series resistances and determine the role of the coulombiennes collisions at low temperature. the application of the model on short shannel, thin gate oxide filn transistors operated from helium to room temperature show a best fit compared with other methods. The model il also used to study the role of the high K.dielectric gate oxide on the mobility.

B/PI.21 DEFECT STRUCTURE OF NEAR–SURFACE LAYER OF CdHgTe CRYSTALS AFTER LAW –ENERGY AR IONS MILLING.

L. Dumanski(a), I. Stefaniuk(a), I. S. Virt(a,c) and M. Kuzma(a); (a) Insitute of Physics,University of Rzeszow, Poland, (b) Section of Experimental Physics, Pedagogical University, Drogobych, Ukraine, (c) Insitute of Biotechnology, University of Rzeszow, Poland

The surface of CdHgTe crystal is very sensitive on chemical, thermal as well as on electron, or ion beam treatment.. Therefore, this material can be used as a very good tester for study the mechanisms and consequences of such processing applied also to other semiconductors. The CdHgTe is a basic material for infrared detectors and these studies will be also important in the engineering of detectors of new generation. The facility of changing of properties of near- surface layer by law- energy ion beam follows from weakness of bindings of Hg atoms in crystal lattice. The Hg vacancies form not only new electrically active defects, but they stimulate the diffusion of impurities and dopants as well. In this paper we study the near -surface layer formed by ion beam milling of n- type CdHgTe crystals . The results of Hall measurements were interpreted basing on considerations of nonhomogenous sample consisting both bulk and layer parts. The model of creation and diffusion of defects is proposed for significant changing of electrical properties of layer. The results point on the possibility of easy control of defect and dopant engineering in thin near-surface layer.

B/PI.22 CHARACTERISATION OF SILICON CARBIDE THIN FILMS GROWN ON Si AND SiO2/Si SUBSTRATES

M. Gelfi(a), E. Bontempi(a), R. Roberti(a), C. Ricciardi(b), G. Barucca(c), L. E. Depero(a) and P.Zanola (a); (a) INSTM and Dipartimento di Ingegneria Meccanica, Università di Brescia, Italy, (b) INFM-Dipartimento di Fisica, Politecnico di Torino, Italy, (c) INFM and Dipartimento di Scienze dei Materiali, Università di Ancona, Italy

Due to its outstanding electrical and mechanical properties, silicon carbide (SiC) is considered a leading semiconducting material for high temperature sensors. Since the piezoresistive effect in SiC is highly anisotropic and exhibits a dependence on the crystal orientation, the role of the substrate on the residual stress must be investigated. This paper presents the structural and morphological characterisation of polycrystalline 3C-SiC films using two-dimensional X-Ray diffraction, AFM and TEM techniques. 3C-SiC thin films were grown on single crystalline Si and on SiO2/Si substrates under the same deposition conditions. The influence of the two substrates on the structural and microstructral properties of the films was investigated. A particular attention was devoted to the stress effects induced in the SiC layers and to the release of the residual strain of the films by extended defects.

B/PI.23 PHYSICAL MODELING OF FERMI-LEVEL EFFECTS FOR DECANANO DEVICE PROCESS SIMULATIONS

P. Castrillo, I. Martin-Bragado, R. Pinacho, M. Jaraiz, J. E. Rubio and J. Barbolla, Dpt. of Electronics, University of Valladolid, Spain

Current decananometer CMOS technology faces complexities arising from the need for very high-doping, reduced thermal budged (non-equilibrium conditions), and 3-dimensional effects. Under such conditions it would be advantageous to be able to directly implement the underlying physical mechanisms. In this work we report on a physically-based Fermi-level modeling approach designed to be accurate and yet appropriate for its implementation in a device-size process simulator. We use an atomistic kinetic Monte Carlo method in conjunction with a continuum treatment for carrier densities. The model includes (i) charge reactions and electric bias according to the local Fermi-level , (ii) pairing and break-up reactions involving charged particles, (iii) clustering-related dopant deactivation and (iv) Fermi level-dependent solubility. Degenerated statistics, band-gap narrowing, and damage-induced electrical compensation are also included. The parameters used for charged particles are in agreement with ab-initio calculations and experimental results. This modeling scheme has proven to be very efficient for realistic device-dimension process simulations. We present an illustrative set of simulation results for common dopants, and discuss the potential of this approach for accurate decanano CMOS device process simulation.

B/PI.24 NEW RESIST CHARACTERISATION: STABILITY TO MB SEMI F21-95 CONTAMINANTS

T. Curro(b), F. Cordiano(b), G. Franco(b), G. Mondio(a) and G. Ippedico(b); (a) Dipartimento di Fisica Sez. Fisica della Materia, Università di Messina, Italy, (b) STMicroelectronics, Catania, Italy

AMC (Airborne Molecular Contamination) effects reveal to be more and more prominent in clean room technology shrinking the dimensions of electronics devices such as last generation flash memories devices (0.15-0.13 micron) .

This works allowed us to evaluate new resist stability in critical conditions, such as basic contamination of clean room environment (~ 20 ppb), higher than a typical contamination status into the equipment (~ 2 ppb). We prove the validity of a theoretical model developed for interpret contaminants adsorption (Sheng-Bai Zhu, Ph.D. “Molecular Contamination on Silicon wafers : A theoretical Study”, Asyst Technologies, Inc.). Then we interpolate critical data between 1 and 5 minutes. The starting shift rate (12 nm/min) exponentially decreases, so we can say that T-Topping is a phenomena almost

instantaneous, in experimental condition (Clean room exposure) 2 minutes are sufficient to obtain CD values higher than specific limits.

Wednesday, May 26, 2004 Afternoon

Session IV: Silicides II
Session chair: T. Clarysse (IMEC, Belgium)

B-IV.1 14:10 -Invited-

FORMATION OF ERBIUM SILICIDE AS SOURCE AND DRAIN FOR DECANANOMETER-SCALE N-TYPE SCHOTTKY BARRIER MOSFETS

M. Jang, Y. Kim, J. Shin and **S. Lee**, Nano-electronic Device Team, Semiconductor and Basic Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon, Korea

In Schottky barrier MOSFETs (SB-MOSFETs), source and drain regions are composed of silicide instead of impurity doped silicon. The structure is quite simple and ultra shallow junction can be formed easily and accurately with low parasitic source and drain resistance. The silicided junction formation temperature is very low in SB-MOSFETs, giving the opportunity to use metal gate and high-k gate insulator. Moreover, the complicated channel doping steps can be eliminated because Schottky barrier exists between junction and channel. Thus, SB-MOSFETs have been proposed as an alternative to the conventional MOSFETs for decananometer-scale application. In this work, erbium is chosen as source/drain metal of n-type SB-MOSFETs, because of its low Schottky barrier height (0.28 eV) for electrons. Erbium silicide is formed on SOI (Silicon-on-Insulator) by using rapid thermal annealing technique. Annealing temperature and time is 500 C and 5 min, respectively. The formation of ErSi1.7 phase is confirmed by x-ray diffraction and Auger electron spectroscopy analysis. Also, the growth mechanisms of ErSi1.7 with the variation of the SOI thickness are investigated and the proper thickness condition between erbium and SOI is determined for the stable growth of ErSi1.7. The sheet resistance of ErSi1.7 is less than 30 ohm/square even if the line width is less than 100 nm. Thus, ErSi1.7 is applicable in decananometer-scale SB-MOSFETs. The manufactured 50 nm gate length n-type SB-MOSFET shows excellent transistor characteristics with large on/off current ratio and low leakage current, which shows the possible applicability of ErSi1.7 as source/drain junction in decananometer-scale n-type SB-MOSFETs.

B-IV.2 14:50

OPTIMIZING THE FORMATION OF NICKEL SILICIDE

J. Foggiato(a), W. S. Yoo(a), T. Murakami(b) and T. Fukada(b); (a) WaferMasters, Inc., San Jose CA, U. S. A., (b) WaferMasters Service Factory, Kumamoto, Japan

The formation of Nickel Silicide has become very important for implementation into sub 100 nanometer technology. Its lower formation temperature and silicon consumption all address the process integration needs for these advanced technologies. Critical to the formation of the low resistivity stoichiometric form of NiSi is the thermal process with the need for uniform temperature and controlled heating of the wafer. A combination of process sequences and parametrics were investigated to achieve more optimal electrical and mechanical characteristics. The electrical resistivity can be optimized through a lower thermal budget process sequence and utilizing multiple step processing. Stress is minimized through allowing the natural heating of the wafer in a resistive based isothermal cavity and multiple step processing. Maintaining the wafer in a constant thermal environment, the heat absorbed by the wafer controls the temperature and thermal energy utilized by the NiSi phase transitions. The optimization methodology will be described including some of the pitfalls that may occur, especially for implementation for advanced technologies in the 65 and 45 nm node. The consumption of silicon is compared with various process sequences to understand the limitations of thermal cycles. Whereas stress is induced by the thermal cycles, the effect of temperature ramping was investigated noting that the final stress is dependent on the film composition and thickness.

B-IV.3 15:10

NANOMETER SCALE CHARACTERISATION OF CoSi2 AND NiSi INDUCED STRAIN IN SILICON BY CONVERGENT BEAM ELECTRON DIFFRACTION

A. Benedetti, H. Bender, C. Torregiani, M. Van Dal and K. Maex; IMEC, Leuven, Belgium

Silicides, an essential component in modern microelectronics, are well known to significantly distort the underlying silicon. This problem is particularly significant for devices well below the 0.1 µm level. Convergent Beam Electron Diffraction (CBED) in the Transmission Electron Microscope is a high spatial resolution method of measuring strain distributions in such structures : if field emission guns are employed, nm-sized electron spots are possible. The components of the strain tensor are obtained through the measurement of the shift of the lines present in the central disk of the diffraction pattern. We have analysed by CBED the strain distribution within the silicon active areas in structures with different channel lengths, down to less than 0.1 µm, surrounded by differently sized stripes of two different silicides, NiSi and CoSi2. In this way, the influence of both composition and size on the underlying silicon can be separately analysed and compared to what predicted by Finite Element simulations. In addition, the problem of interpreting CBED patterns exhibiting split diffraction lines, which originate at shallow depths below the silicide/silicon interface, is critically assessed and an explanation proposed.

B-IV.4 15:30

EXPLORING Ni-Si THIN-FILM REACTIONS BY MEANS OF SIMULTANEOUS SYNCHROTRON X-RAYS DIFFRACTION AND SUBSTRATE CURVATURE MEASUREMENTS

C. Rivero(a), P. Gergaud(a), M. Gailhanou(b), B. Froment(b) and O. Thomas(a); (a) TECSEN, Univ. Aix-Marseille III, France, (b) LURE, Univ. Paris Sud, Orsay, France

15:50 **BREAK**

Session V: Laser annealing
Session chair: T. Feudel (AMD, Germany)

B-V.1 16:10 -Invited-

THE EUROPEAN ANSWER TO THE INTEGRATION ISSUES OF EXCIMER LASER ANNEALING IN MOS TECHNOLOGY

V. Privitera(a), A. La Magna(a), G. Fortunato(b), M. Camalleri(c), A. Magrì(c), F. Simon(d) and B. G. Svensson(e); (a) CNR-IMM, Catania, Italy, (b) CNR-IFN, Roma, Italy, STMicroelectronics, Catania, Italy, (d) MicroLas Lasersystem, Gottingen, Germany, (e)Department of Physics, University of Oslo, Norway

Excimer laser annealing (ELA) of MOSFET devices is currently studied and evaluated within the frame of the IST project FLASH (Fundamentals and applications of laser processing for highly innovative MOS technology), funded by the European Commission. We want to prove, as a final aim of the project, that ELA can be industrialized in the context of semiconductor device fabrication. Therefore, after testing the feasibility of the process on specimens, the consortium is pursuing the irradiation of entire wafers by an industrial line beam system setup for 405mm line length and 400µm line width, driven by a Lambda Physik LS2000 laser. Shallow junctions (~80 nm), characterized by sheet resistance values of 90 Ohm/ with standard deviation of 2.8 % on wafer, relative to low energy implants treated by ELA, have been obtained with industrial equipment. Furthermore, from the microscopic analysis of a gate stack integrated with several possible solutions to avoid the detrimental effects of the laser beam on device structures, we studied how to tackle the integration issues, main obstacles for the use of ELA in the semiconductor industry. The launch of ELA, to open a new market segment in the semiconductor industry, implies the availability of reliable process simulation tools. Therefore, we produced a simulation program based on an analytical approach, fully working and available.

B-V.2 16:50

REAL-TIME MODELING OF EXCIMER LASER ANNEALING OF ULTRA-SHALLOW DOPING

J.-Y. Degorce, J.-N. Gillet, Y. Liao and M. Meunier; Laser processing Laboratory, Ecole Polytechnique de Montreal, Canada

Ultra-shallow junctions, which are essential to continue the down-scaling in CMOS technologies, require fast and high temperature annealing to increase dopant activation and remove implantation defects. Among the various annealing processes, the one using an excimer laser presents the advantages over conventional annealing of being very fast and localised only at the surface, thus limiting the thermal budget of the substrate. We introduced a single equation for modeling both diffusion and segregation phenomena over the whole material (i.e. solid and melt) in laser induced ultra-shallow doping process. From our simulation, we showed that for any preset implanted doses in silicon and maximal molten depths, all dopant profile converge after only few laser pulses to a distribution that only depends on the diffusion coefficient D and segregation coefficient k of the dopant in the liquid phase. A perfect box-like profile can only be reached for dopants presenting no liquid-solid segregation (i.e. k = 1), which is roughly the case for boron. However, when the segregation is stronger as for phosphorous (k=0.35) and arsenic (k=0.3), the junctions become shallower and in the limiting case of k close to 0 as for In (k=0.004), all dopants agglomerate at the bulk surface over a thickness of few nm for an initial distribution of 80 nm. From these simulations, experimental determinations of the segregation coefficient k have been made possible, which only requires experimental knowledge of the annealed profile and diffusion coefficient of the dopant.

B-V.3 17:10

COMPUTATIONAL METHODS FOR THE SIMULATION OF THE EXCIMER LASER ANNEALING IN MOS TECHNOLOGY

A. La Magna(a), P. Alippi(a), V. Privitera(a), G. Fortunato(b), L. Mariucci(b) and M. Camalleri(c); (a) CNR-IMM, Catania, Italy, (b) CNR-IFN, Roma, Italy, (c) STMicroelectronics, Catania, Italy

The integration of the laser annealing process in MOS technology requires predictive codes for the simulation of the material modification due to the interaction between the laser radiation and the structure itself. These computational tools have a twofold aim, i.e. a) the estimate of the heat sources space distribution in the specimen and b) the simulation of the phenomena occurring inside the specimen during the irradiation (thermal field evolution, melting and re-growth of localised zones, dopant redistribution). Our modelling methodology is based on coupled finite-difference-time-domain and phase-field methods, applied to the simulation of the irradiation and the structural evolution respectively. We considered as simulation framework typical MOS structures, i.e. the implanted impurity profiles in two dimensional samples containing also metal/SiO2/a-Si/c-Si stacks. The model is calibrated for the cases of different impurity atoms also using the outcomes of molecular dynamics simulations. Our results, validated by experimental characterisations of laser annealed samples, demonstrate the necessity of a complete numerical approach. In particular, the effects of the device geometry and the optical/thermal properties of the material used are discussed in detail.

B-V.4 17:30

LASER THERMAL PROCESSING USING AN OPTICAL COATING FOR ULTRA SHALLOW JUNCTION FORMATION

M. Hernandez(a), J. Venturini(a), G. Kerrien(b), T. Sarnet(b), D. Débarre(b), J. Boulmer(b), C. Laviron(c), D. Camel(c), J.-L. Santailler(c) and H. Akhouayri(d); (a) SOPRA, Bois Colombes, France, (b) IEF, Université Paris-Sud, Orsay, France, (c) CEA-G/LETI, Grenoble, France, (d) Institut Fresnel, Marseille, France

Semiconductor doping is a critical step in microelectronic device fabrication. Particularly, ultra-shallow junction formation for the CMOS 45nm node is today intensively studied. Laser Thermal Processing (LTP) has already shown potentiality to achieve abrupt and ultra-shallow junctions, with a very low resistivity. However, the laser process has to be integrated in the conventional process flow of a real CMOS device fabrication. Therefore, the laser treatment needs to preserve the integrity of the different irradiated structures like transistor gates. Optical coatings, including reflective and anti-reflective layers, can be used to protect the structures and to control the lateral diffusion of the dopants. In this work, we have studied different optical coatings (different materials and thicknesses) with two different excimer lasers at 308 nm: a long pulse SOPRA VEL 15 (200ns-15J) and a Lambda Physik Compex (20 ns-200 mJ). Junctions have been characterized by Secondary Ion Mass Spectroscopy, 4-point probe, Infra-Red Spectroscopic Ellipsometry, in-situ reflectivity and UV photometry. The efficiency and the integrity of the different coatings have been studied for different laser irradiation conditions in solid and molten phase. The results show that a proper

optical coating optimizes the coupling of the deposited laser energy and is promising for improving the integration of the laser activation process of future CMOS junctions.

B-V.5 17:50

SURFACE MORPHOLOGIES OF EXCIMER-LASER ANNEALED BF2+ IMPLANTED Si DIODES

A. Burtsev(a), L. K. Nanver(a), A. van Veen(b), H. Schut(b), J. Slabbekoorn(a) and T. L. M. Scholtes(a); (a) Laboratory of Electronic Components, Technology and Materials (ECTM), Delft Institute of Microelectronics and Submicron Technology (DIMES), Delft University of Technology, The Netherlands, (b) Interfaculty Reactor Institute (IRI), Delft University of Technology, The Netherlands

Excimer laser annealing (ELA) of implanted dopants has been identified as one of the only means of forming ultra-shallow junctions for future CMOS generations. The heavy BF_2^+ ion, rather than pure B^+, is often used to effectively reduce the B implantation energy, as well as to both reduce channeling and implantation time. We have previously demonstrated near ideal p^+-n Si diodes formed by 5 keV BF_2^+ implantation directly followed by laser annealing at energies between 900-1100mJ/cm^2 [1]. Junction depths of 20 - 30 nm and abruptness values down to 1.5 nm at 10^{18} cm^{-2} were achieved.

In this paper the laser-induced Si surface roughness is shown to be comparable to and may even exceed the junction depth. The surface roughness of such diodes has been studied for a wide range of laser energies, by using techniques such as AFM, SEM, TEM and Positron Beam Analysis (PBA). It is found to increase with laser energy density, and reaches a value of 3.6 nm after ELA at 1200 mJ/cm^2. However, anomalous behavior is witnessed at 800 mJ/cm^2, at which energy very high surface protrusions up to 9 nm high are observed. By PBA this behavior is correlated to extensive cavity formation in the Si whereby the volatile F_2 fraction can accumulate and evaporate, leading to Si surface bubbling. The consequences for the diode characteristics and contact resistivity are examined.

[1] L.K. Nanver, J. Slabbekoorn, A. Burtsev, *et al*., ECS Proceedings 2003, **Vol. 14**, pp. 119-130.

B-V.6 18:10

BORON-ENHANCED DIFFUSION IN EXCIMER LASER ANNEALED Si

E. V. Monakhov(a), B. G. Svensson(a), M. K. Linnarsson(b), A. La Magna(c), C. Spinella(c), C. Bongiorno(c), V. Privitera(c), G. Fortunato(d) and L. Mariucci(d); (a) Department of Physics, Physical Electronics, University of Oslo, Norway, (b) Solid State Electronics, Royal Institute of Technology, Stockholm, Sweden, (c) CNR-IMM, Catania, Italy, (d) CNR-IFN, Roma, Italy

The effect of excimer laser annealing (ELA) and rapid thermal annealing (RTA) on B redistribution in B-implanted Si has been studied by secondary ion mass spectrometry (SIMS) and spreading resistance probe (SRP). B has been implanted with an energy of 1 keV and a dose of 1e16 cm-2 creating a distribution with a width of 20-30 nm and the peak concentration of ~5e21 cm-3. It has been found that ELA with 10 pulses of the energy density of 850 mJ/cm2 results in a uniform B distribution over the ELA-molten region with an abrupt profile edge. SRP measurements demonstrate good activation of the implanted B after ELA, with the concentration of the activated fraction (~1e21 cm-3) exceeding the solubility level. RTA (30 s at 1100oC) of the as-implanted and ELA-treated samples leads to a diffusion of B with diffusivities exceeding the equilibrium one and the enhancement is similar for both of the samples. It is found that RTA results also in reduction of the activated B in the ELA-treated sample to the solid solubility (2e20 cm-3). The similarity of the B diffusivity for the as-implanted and ELA-treated samples suggests that the enhancement of the B diffusivity is due to the so-called boron-enhanced diffusion (BED). Possible mechanisms of BED are discussed.

Thursday, May 27, 2004 Morning

Session VI: Silicon processing I
Session chair: V. Privitera (CNR-IMM Catania, Italy)

B-VI.1 08:30 -Invited-

ADVANCED FRONT-END PROCESSES FOR THE 45 NM CMOS TECHNOLOGY NODE

E. J. H. Collart(a), S. B. Felch(a), H. Graoui(a), S. Tallavarjula(a), R. Lindsay(b), B. J. Pawlak(c), J. A. Van den Berg(d), N. E. B. Cowern(e) and K. J. Kirkby(e); (a) Front End Products Group, Applied Materials Inc., Sunnyvale CA, U. S. A., (b)IMEC, Leuven, Belgium, (c) Philips Research Leuven, Leuven, Belgium, (d) Joule Physics Laboratory, School of Sciences, University of Salford, U. K., (e) Advanced technology Institute, School of Electronics and Physical Sciences, University of Surrey, U. K.

Co-implantation (also called cocktail) implants for junctions extensions are proven experimentally to be very attractive and currently receiving a lot of attention, particularly for p-type implants. The effect of combining different species with B such as F and Ge will be discussed in terms of improved activation, abruptness and junction depth. The optimum combination of Ge pre-amorphization with F co-implantation provides beneficial B diffusion in the amorphous phase of Si at the level of 2e20 at/cm3 with abrupt tail due to efficient F mediated suppression of B transient enhanced diffusion. An interesting option for very shallow and well defined n-type implants is using Sb. The high mass (AMU121) assures narrow, and abrupt dopant profiles. The activation and diffusion behaviour under conditions compatible with 45 nm technology requirements will be discussed. An additional route to improved transistor performance are Silicon-On-Insulator (SOI) substrates. Initial results of a comparison between bulk and thin SOI (550A) will be presented, focusing on the regrowth characteristics after Ge pre-amorphisation implants and EOR damage evolution. Advanced annealing dopant activation techniques, such as sub-melt non-melting laser annealing, with maximum temperature dwell times of about one millisecond are being developed. They enable above solid solubility dopant activation with dramatically suppressed minimal diffusion in comparison to the as-implanted dopant profile. Nevertheless, achieving low sheet resistances with junctions formed by these advanced anneals is a challenge, but careful optimization of the pre-amorphisation, co-implant and dopant implant conditions enables the formation of p+-n junctions that come very close to satisfying the ITRS 45 nm requirements.

B-VI.2 09:10

NITROGEN INTERACTION WITH VACANCIES IN SILICON

V. V. Voronkov(a) and R. Falster(b); (a) MEMC Electronic Materials, Merano, Italy, (b) MEMC Electronic Materials, Novara, Italy

In nitrogen-doped Float-Zoned crystals vacancies are trapped by single nitrogen interstitials, in the form of a VN species (substitutional nitrogen atoms). They are thus prevented from agglomeration into voids. The VN species are known to be deep centres. The deep centres have been reported in nitrogen-doped samples but only after annealing and quenching. A model to account for this and some other observations is presented. The main point is that apart the 'conventional' monomeric/dimeric nitrogen community, N1/N2, there is another monomeric species N1* that does not pair into N2 but that is entirely responsible for the interaction with vacancies. Upon cooling, this species traps a free vacancy to become a VN deep centre. At still lower T, it traps one more N1* atom to become VN2. During subsequent annealing, VN2 is returned to the initial VN form and can be frozen-in if the cooling rate is sufficiently high. With longer anneals, the N1* atoms (vacancy traps) are lost by precipitation resulting in a fast vacancy out-diffusion. This model also provides an explanation for reported peculiarities of vacancy conversion into substitutional platinum (Pts) by a Pt diffusion test. The 'countable' species is VN2. By pre-annealing, the concentration of N1* atoms is strongly reduced, and the subsequently counted vacancy concentration will be limited by the small amount of the N1* atoms: all of them will be trapped by VN and give rise to Pts and N2 dimers.

B-VI.3 09:30

INDIUM DIFFUSION AND ACTIVATION IN SILICON: EXPERIMENTS AND THEORETICAL INVESTIGATIONS.

P. Alippi, S. Scalese, A. La Magna and V. Privitera, CNR-IMM Catania, Italy

Indium is considered as an alternative to boron as p-type dopant in silicon: although showing lower electrical activity, it allows the realization of steeper as-implanted profiles, due to its heavier mass. Increased activation is found in samples co-implanted with carbon, presumably due to the shallow electronic level associated to In-C complex. In this work, we first present the results of a systematic experimental study on indium implantation in silicon, performed over a large range of implant energies and doses. The effects of C (present in the silicon substrate either as a contaminant or as co-implanted species) on In activation and diffusion are investigated. In order to fill the lack of theoretical investigations on In-related defects in Si, we then provide a well founded ab-initio picture of defect energetics and diffusivity over which a continuum diffusion model is built. Equilibrium structures of In complexes with Si defects, vacancy (V) and interstitials (I), and with C impurities, are investigated within density functional theory, using the Vienna Ab-initio Simulation Package. We determine migration energies of the I- and V-mediated diffusion mechanisms, locating the saddle points along the minimum energy paths. We identify the In-C complex responsible for increased electrical activation in co-implanted samples and discuss its formation mechanism. The ab-initio energetics is then integrated into a continuum diffusion model, allowing a direct comparison with experimental data. The diffused profiles obtained by the simulations are compared to those measured by secondary-ion-mass-spectroscopy after implantation and thermal annealing, showing a noteworthy agreement at different process conditions.

B-VI.4 09:50

THEORY OF NATIVE-DEFECT ASSISTED DIFFUSION OF THE B, Al, Ga, AND In ACCEPTORS IN SILICON

G. Lopez(a), C. Melis(a), P. Schirra(a), P. Alippi(b) and V. Fiorentini(a); (a) Dept. of Physics, University of Cagliari, Italy, (b) IMM-CNR, Catania, Italy

We present a complete picture of the diffusion of acceptors in silicon based on ab initio density-functional-based calculations [1] on the structure, extrinsic levels, formation and migration energies of the B, Al, Ga, and In acceptors in crystalline Si, and of their complexes with vacancies and self-interstitials. These complexes are known to be responsible for the transient enhancement of dopant diffusivity [2] in Si, a key issue in the formation of ultrashallow junctions in Si-based CMOS integrated circuit technology. We find self-interstitial assisted diffusion to be preferred over vacancy-assisted mechanisms in all cases, although the two become competitive as the acceptor increases in size. The ground state of the complexes is unexpected and "anomalous" in several cases: Al and In coupled to a vacancy go off-site forming a divacancy-intertitial complex; the standard self-interstitial/acceptor complex predicted for B is unstable for Al and Ga, which are ejected in the interstitial region and are electrically deactivated as acceptors.

1. M. Payne et al., Rev. Mod. Phys. 64, 1045 (1992) 2. Material Research Society Bulletin 25, No. 6, Special Issue on Defects and Diffusion in Silicon Technology (2000); especially N. Cowern and C. Rafferty, p.39.

B-VI.5 10:10

COMPREHENSIVE, PHYSICALLY BASED MODELLING OF As IN Si

R. Pinacho, M. Jaraiz, P. Castrillo, J. E. Rubio, I. Martin-Bragado and J. Barbolla, Dpt. of Electronics, University of Valladolid, Spain

An accurate knowledge of the behaviour of As appearing at high concentrations during thermal processes is essential for today's CMOS technology so that As is the most widely used Si dopant in ultralarge scale integrated circuits. In spite of the large amount of successful research work devoted to reproducing As kinetics in Si, the level of complexity reached by Si device fabrication technologies claims for a more comprehensive physical modelling that, based on fundamental parameters of some basic As configurations could simultaneously account for aspects such as diffusion, electrical deactivation and amorphization after As implantation among others. We have used the atomistic kinetic Monte-Carlo simulator DADOS to develop a consistent physical model for As that includes a limited set of AsV clusters of different sizes and energies. Through a detailed modelling of Fermi level effects, we will discuss the main features of As behaviour in Si such as (i) intrinsic and extrinsic As diffusion, (ii) electrical deactivation at high As concentrations (iii) annealing of As implantated profiles and (iv) other striking features such as the interstitial supersaturation induced by rapid electrical deactivation of very high As concentrations at low temperatures.

10:30 **BREAK**

Session VII: Silicon processing II
Session chair: J. Van den Berg (University of Salford, U.K.)

B-VII.1 10:50 -Invited-

MAINSTREAM RAPID THERMAL PROCESSING FOR SOURCE DRAIN ENGINEERING FROM FIRST APPLICATIONS TO LATEST RESULTS

J. Niess, S. Paul, S. Buschbaum and W. Lerch; Mattson Thermal Products GmbH, Dornstadt, Germany

Rapid thermal processing (RTP) technology has been commercially available in the semiconductor industry for about 30 years. Already in 1957, e.g., a solar furnace with a parabolic Al reflector was designed. Despite of this it took several tens of years until RTP of semiconductors penetrated the market. In the meantime, RTP has become a mature application. As a replacement of standard furnaces, it proves outstanding ambient control and very short heating cycles with highest ramp rates for suppression of unintended processes like diffusion, surface degradation, and others but maintaining desired processes like, e.g., implant activation, silicide formation or oxide growth. In the field of ultra shallow junction (USJ) formation, which is necessary to avoid short channel effects arising during continued scaling of CMOS devices RTP is indispensable. With the introduction of CoSi2 as source drain contact material and its transition to NiSi for future technology nodes RTP delivers unique features in terms of ambient control, single wafer processing and others. In the current paper we will present the development and potential of RTP throughout this era and show latest results in USJ annealing as well as source drain contact formation down to the 90 nm and 65 nm technology node of the ITRS2003, respectively.

B-VII.2 11:30

PHYSICALLY BASED MODELLING OF DAMAGE, AMORPHIZATION, AND RECRYSTALLIZATION FOR PREDICTIVE DEVICE-SIZE PROCESS SIMULATION

J. E. Rubio, M. Jaraiz, I. Martin-Bragado, R. Pinacho, P. Castrillo and J. Barbolla, Dept. of Electronics, University of Valladolid, Spain

Current advanced CMOS source/drain engineering involves the use of amorphizing implants with 3D geometry. Upon annealing, the induced transient enhanced diffusion (TED) can only be accurately predicted if the amorphized region is correctly modelled, as well as the formation and evolution of extended defects, like 311's and dislocation loops. In addition to extended defects, already modelled in DADOS, we have developed a physically based modelling approach for the implant-induced damage build-up, amorphization and recrystallization suitable to handle device-size process simulation. It is based on amorphous pockets (agglomerates of an arbitrary number of interstitials and vacancies, plus trapped impurities) with size-dependent activation energy. The model reproduces many experimental aspects like the crystal-amorphous transition temperature as a function of dose rate and ion species, and the superlinear increase of damage with dose. We discuss the model with simulation examples of several common impurities. The efficiency of the model, in terms of CPU time and memory requirements, will also be shown.

B-VII.3 11:50

MODELING AND CHARACTERIZATION OF ATOMICALLY SHARP "PERFECT" Ge/SiO2 INTERFACES

W. Windl(a), T. Liang(a), S. Lopatin(b) and G. Duscher(b,c); (a) The Ohio State University, Columbus OH, U. S. A., (b) North Carolina State University, Raleigh NC, U. S. A., (c) Oak Ridge National Laboratory, Oak Ridge TN, U. S. A.

We have studied the atomic structure of the interface between Ge and SiO2 using a combination of materials simulations based on density functional theory with atomic-resolution Z-contrast imaging and electron

energy-loss spectroscopy (EELS). The comparison of the theoretical with the experimental results, especially from EELS, which was pushed to atomic resolution for the first time in this study, are consistent with the model of an atomically abrupt, “ideal” Ge/SiO2 interface, which has been not observed in the past, not even for the case of Si/SiO2 interfaces. This is even more surprising considering that the examined sample has been fabricated two decades ago by oxidation of Ge-implanted Si. There, Ge was expelled from the growing oxide and piling up in front of the oxidation front, similar to snow in front of a snowplow (hence the nickname "snowplowing"), until the Ge concentration reached ~100%. Although at the time the interface has been noted to be very flat, an accurate characterization of its structure has been lacking to date. Our results indicate the potential both for a more successful use of germanium in high-speed devices (it is shown to form an excellent interface with oxides) and for a way to improve interface engineering to enhance performance in electronic devices. Ab-initio based Monte Carlo modeling of the snowplowing process suggests that the undesirable electrical properties that sometimes occur with devices containing Ge might be due to Ge incorporation into the oxide.

B-VII.4 12:10

PHASE FIELD MODEL FOR THE DOPANT REDISTRIBUTION DURING SOLID PHASE EPITAXIAL REGROWTH OF AMORPHIZED SILICON

C. Zechner, D. Matveev and A. Erlebach, ISE Integrated Systems Engineering AG, Zurich, Switzerland

Silicon regions amorphized by high dose ion implantation recrystallize under high temperature treatment. Driven by a lower configuration energy of dopant atoms in the amorphized phase than in the crystalline phase, dopant atoms are pushed in the direction of recrystallization during solid phase epitaxial regrowth (SPER). An accurate model for this effect is important for a correct simulation of dopant profiles and surface dose loss in deep sub-micron technology. In this work, a phase field, which describes the crystallinity of silicon, is introduced for the modeling of SPER. The time evolution of this phase field during SPER is described by a partial differential equation. The gradient of the crystallinity field acts as a driving force for dopant drift during SPER. The simulation results are in excellent agreement with As, In, and F SIMS data, which monitor the redistribution of dopants during and after SPER.

B-VII.5 12:30

MECHANISMS OF BORON-INTERSTITIAL-CLUSTERS FORMATION AND DISSOLUTION AT HIGH B CONCENTRATION

D. De Salvador(a), S. Mirabella(b), E. Napolitani(a), G. Bisognin(a), L. Aldegheri(a), E. Bruno(b), G. Impellizzeri(b), A. V. Drigo(a), M. Berti(a), A. Carnera(a) and F. Priolo(b); (a) INFM and Dipartimento di Fisica, Università di Padova, Italy, (b) MATIS - INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Italy

The scaling-down of Si microelectronic devices requires progressively high active B content in narrow layers, mainly obtained by B implantation. The excess of interstitial (I) defects, produced by ion implantation, causes a boron-interstitial co-precipitation in immobile and electrically inactive clusters (named BICs), which deteriorate the electrical properties of devices. We have investigated the BICs formed in a thin epitaxial boron box (10^19 and 10^20 B/cm^3), after 20 keV Si implantations in a Si cap covering the box and subsequent annealings. By means of secondary ions mass spectrometry measurements of B profiles of the box and of three buried B-delta dopings and by a proper modeling of B diffusion, we have estimated the B and I doses trapped in the BICs, both after their formation and during their subsequent dissolution at different temperatures. BICs formed at the low box concentration (10^19 B/cm^3) have a B:I stoichiometric ratio of about 1:1, while the main mechanism of their dissolution is by B interstitialcy (BI) release. At 10^20 B/cm^3 B box concentration new mechanisms prevail: BICs are much poorer in interstitials (B:I≈3:1) and BICs dissolution proceeds through the emission of a B mobile species having a much longer mean free path (tens of nm) than the usual BI mobile species. On the basis of recent theoretical works, this has been interpreted as the emission by the BICs of a mobile B2I species, opening a new scenario in the BICs dissolution dynamics.

12:50 **LUNCH**

Thursday, May 27, 2004 Afternoon

Session VIII: Ultra shallow junctions
Session chair: F. Priolo (Università di Catania, Italy)

B-VIII.1 14:10 -Invited-

ACCURATE ELECTRICAL ACTIVATION CHARACTERIZATION OF CMOS ULTRA-SHALLOW PROFILES

T. Clarysse(a), F. Dortu(a), R. Loo(a), W. Vandervorst(a,b), B. J. Pawlak (c) and C. Defranoux(d); (a) IMEC, Leuven, Belgium, (b) KU Leuven, Electrical Engineering Dept., INSYS, Leuven, Belgium, (c) Philips Research Leuven, Leuven, Belgium, (d) SOPRA, Bois-Colombes, France

Understanding dopant diffusion and activation mechanisms is a key issue for future sub-45 nm CMOS technologies. This understanding requires the availability of accurate chemical and electrically active dopant profiles. In this work we will focus on the accurate characterization of the electrical active portion of ultra-shallow junction (USJ) profiles, including a precise sheet resistance determination. We will discuss the pro's and contra's of respectively, electrical depth profiling by the Spreading Resistance Probe (SRP), sheet resistance measurements with low weight Four Point Probe (FPP) systems and alternative solutions based on probe-spacing experiments with an SRP-tool, and electrical characterization by non-destructive, optical techniques such as Carrier Illumination (CI) and Infra-Red Spectroscopic Ellipsometry (IR-SE). The comparison will be based on state-of-the-art structures such as steep 1-2 nm/decade, sub-50 nm depth, Chemical Vapor Deposition (CVD) layers with different thicknesses and dopant levels, before and after different annealing cycles (with only slightly different activation levels and dopant out-diffusions) and Solid Phase Epitaxially Regrown (SPER) source-drain structures, including the impact of post-annealing cycles on the electrical activation. It will be illustrated that electrical characterization can supply essential information not otherwise obtainable through other means such as Secondary Ion Mass Spectrometry (SIMS) chemical profiling.

B-VIII.2 14:50

THERMAL STABILITY OF BORON ELECTRICAL ACTIVATION IN PRE-AMORPHISED ULTRA-SHALLOW JUNCTIONS

F. Cristiano(a), N. Cherkashin(a), P. Calvo(a), Y. Lamrani(a), X. Hebras(a), A. Claverie(a) and W. Lerch(b) and S. Paul(b); (a) Pôle Implantation Ionique CEMES/LAAS-CNRS, Toulouse, France, (b) Mattson Thermal Products, Dornstadt, Germany

Boron implantation into pre-amorphised silicon followed by Solid Phase Epitaxial Growth (SPEG) at low temperature (<700°C) represents a promising doping method to meet the requirements for source/drain junctions in future device technologies. This technique allows very high activation levels (above equilibrium solid solubility) with minimum dopant diffusion (due to the very low thermal budget). However, the activation levels achieved by SPEG appear to be metastable with respect to the subsequent "post-annealing" steps that follow the junction formation in a typical CMOS process flow. In this work, we present a detailed study of the thermal stability of activated junctions as a function of the post-annealing conditions. p+/n junctions were formed by implanting 500 eV boron (1x1015 cm-2) into Ge+ preamorphised Si followed by SPEG at 650°C. Post-annealing temperatures ranged from 250 to 950°C, with times ranging from 3 to 1800 seconds. Four point probe (4PP), SIMS and TEM analysis were then used to investigate the evolution of boron activation, boron diffusion and of the implantation induced extended defects. During isothermal anneals in the 750-900°C range, it is found that the sheet resistance initially increases (deactivation) and then decreases (reactivation) with rates proportional to the temperature itself. TEM results elucidate the crucial role of the extended defects in the deactivation process. On the other hand, the combination of 4PP and SIMS measurements allows to separate the respective contribution of both cluster dissolution and dopant indiffusion to the reactivation process.

B-VIII.3 15:10

APPLICATION OF SELECTIVE EPITAXY FOR FORMING OF ULTRA SHALLOW SiGe-BASED JUNCTION

H. Radamson, Royal Institute of Technology (KTH), Department of Microelectronics and Information Technology (IMIT), Kista-Stockholm Sweden

Scaling of CMOS transistor structures demands formation of further shallower source/drain (S/D) junctions. This requires also a low series resistance, which yields to an increase of the S/D doping levels. Incorporation of Ge into Si offers the possibility to increase the dopant concentration in the layer and hence decrease the resistivity. This can be applied to replace the conventional implanted S/D junctions, which are limited in terms of contact resistivity and lateral abruptness. In this work, selective growth of B-, P- or As-doped Si1-xGex structures (0.14<x<0.33) on patterned substrates aimed for source/drain ultra shallow junctions was investigated. The integration issues e.g. pattern dependency (loading effect) and control of doping level were also tackled. By optimizing the growth parameters the surface roughness of these structures was reduced. The results demonstrated that the growth rate enhanced in presence of B in SiGe meanwhile it decreased for the P- or As-doped layers. The amount of Ge was constant for B-doped samples and decreased for As- or P-doped SiGe layers. Abrupt dopant profiles with a good epitaxial quality and low sheet resistances e.g. 195 ohm/square and 260 ohm/square for 420 Å-thick B-doped Si0.81Ge0.19 and P-doped Si0.71Ge0.29 layers were obtained, respectively. The samples were grown on Si [100] substrates in a reduced pressure chemical vapor deposition (RPCVD) reactor at 20 torr. The layers were analysed by secondary ion mass spectroscopy (SIMS), high-resolution reciprocal lattice mapping (HRRLM), atomic force microscopy (AFM) and cross-sectional transmission electron miscopy (XTEM).

B-VIII.4 15:30

SELECTIVE SiGe EPI FOR ULTRA-SHALLOW JUNCTION FORMATION

A. V. Samoilov and Y. Kim, Applied Materials, Front Ent Business Product Group, U. S. A.

Selective SiGe Epi is a very promising technology for forming ultra-shallow junctions in PMOS devices. The main benefits are a) creating local strain in the channel to increase hole mobility; b) high boron activation and

low resistance; c) abrupt boron profiles. Among the challenges of the SiGe deposition is the requirement of selectivity, i.e., SiGe should be deposited on the Si areas only, with no deposition on the dielectric areas. We report in this paper results of heavily boron doped SiGe deposition that is completely selective, compatible with advanced node device manufacturing, with resistivity down to 0.8 mOhm cm (equivalent to 400 Ohm at 20 nm), boron activation of as deposited films above 90% and boron profile abruptness of <3 nm/dec.

15:50 **BREAK**

16:10 **POSTER SESSION II**

B/PII.01

POINT DEFECTS INTERACTION WITH EXTENDED DEFECTS AND IMPURITIES IN Si AND SiO_2

D. Kropman(a), U. Abru(b), T. Kärner(c), Ü. Ugaste(d) and E. Mellikov(e); (a) Estonian Maritime Academy, Tallinn, Estonia, (b) Tondi Electronics, Tallinn, Estonia, (c) Tartu University, Tartu, Estonia, (d) Pedagogical University, Tallinn, Estonia, (e) Technical University, Tallinn, Estonia

The diminishing of the sizeof integrated cicuit elements results in an increasing influence of point defects(PD)on their electrical parameters and reliability.The purpose of the present work is investigation of the dependence of PD generation kinetics on the oxidation condition and its influence on some structural and electrophysical parameters of the Si-SiO_2 system by means of Electron Paramagnetic Resonans (EPR) and surface photo- voltage (SPV) spectra measurements.It has been shown that the vacancies type defects EPR signal intensity dependence on the oxidation time is non-monotonous.This allows to suggest that PD interaction with extendet defects and impurities occur in the Si-SiO_2 system. It has been established that depending on the oxidation condition (time,ambient)the EPR and SPV (0,49eV)signals decrease or increase simultaneously.Surface state Ec-0,49 eV are identified as interstitial Si atoms.This allows to suggest that decrease of EPR and SPV signals are connected with interaction between vacancies and interstitial Si atoms at the interface,while the increase of these signals indicated that vacancies and interstitials atoms are separated and interaction between them is absent.

B/PII.02

ELECTRICAL FINGERPRINT OF PIPELINE DEFECTS

I. Mica, M. L. Polignano and C. De Marco, STMicroelectronics, Agrate Brianza, Italy

These defects consist of a dislocation-induced resistive path and are due to an anomalous dopant diffusion along the defect. Dislocations develop during the device fabrication processes because of the stress in silicon induced by the oxidations of the STI and because of the implantation damage. These defects can reduce device yield either by affecting the devices functionality or by increasing the current consumption under stand-by conditions. So it is very interesting to characterize electrically the pipeline defects. In this work the electrical fingerprint of these dislocations is studied, with the purpose to allow the identification of such defects as the responsible for device failure. Pipeline defects are responsible for a leakage current from source to drain in the transistors. This leakage has a resistive characteristic and it is lightly modulated by the body bias. First, we characterized the leakage current versus temperature and we found that it isn't sensitive to the temperature. Vice versa the off-current of a good transistor exhibits the well-know exponential dependence on 1/T. Then the emission spectrum of these defects was studied and compared with the spectrum of a good transistor. Whereas the spectrum of a good transistor under saturation conditions is characterized by a broad spectral light emission distribution, the leaky one shows a well defined peak at low energies.

B/PII.03

ELECTRONIC LEVELS OF INTERSTITIAL CARBON AND CARBON-OXYGEN CENTERS IN SIGE ALLOYS

J. Coutinho(a), A. Balsas(a), V. J. B. Torres(a), P. R. Briddon(b) and M. Barroso(c); (a) Department of Physics, University of Aveiro, Portugal, (b) School of Natural Sciences, University of Newcastle upon Tyne, U. K., (c) Department of Physics, University of Aveiro, Portugal

The structural and electronic properties of interstitial carbon (C_i) and interstitial carbon-oxygen (C_iO_i) complexes in Si-rich SiGe alloys is studied by ab-initio modeling. A comparison between the electrical activity of both defects allows us to estimate accurate level locations. In the alloys, we find that the donor level of the C_iO_i complex approaches the valence band top, becomes resonant at about $x=0.5$ (where x is the fractional Ge content), and the shift rate corroborates recent photoluminescence measurements. We also discuss the origin for the level shift in terms of volumetric and chemical effects.

B/PII.04

HIGH RESOLUTION DEEP LEVEL TRANSIENT SPECTROSCOPY AND PROCESS-INDUCED DEFECTS IN SILICON

J. H. Evans-Freeman, D. Emiroglu and K. D. Vernon-Parry, Department of Electrical Engineering and Electronics, UMIST, Manchester, U. K.

High resolution, or Laplace, Deep Level Transient Spectroscopy (LDLTS) enables the identification of very closely spaced energetic levels in a semiconductor bandgap. DLTS may resolve peaks with a separation of tens of electron-volts, but LDLTS can resolve defect energy separations as low as a few meV. In this paper we present results from LDLTS when applied to ion-implantation induced defects in silicon, with particular emphasis on characterisation of small extended defects. Silicon was implanted with a variety of ions from mass 28 to 166. A combination of LDLTS and direct capture cross section measurements was employed to show that electrically active small extended defects were present in the as-implanted samples. Larger dislocations were then generated in Si by either oxygenation or stress. These extended defects had typical lengths of microns, and their electrical activity was subsequently characterised by LDLTS. This was to establish the sensitivity of LDLTS to defects whose carrier capture is characterised by a non-exponential filling process, and an evolving band structure as carrier capture proceeds.

B/PII.05

FORMATION OF THERMAL VACANCIES IN HIGHLY N-TYPE SILICON

V. Ranki and K. Saarinen, Laboratory of Physics, Helsinki University of Technology, Finland

The thermal vacancies in Si have escaped the direct experimental observation, despite their fundamental and technological importance. Hence their basic thermodynamical properties such as the formation enthalpy have been unknown. We have studied the formation of thermal vacancies in highly As and P-doped Si using positron lifetime and Doppler broadening measurements. The Czochralski-grown Si(111) bulk crystals with 10^{20} cm^{-3} doping concentration were subjected to isochronal and isothermal annealings at temperatures between 300 K and 1220 K. We observed a clear increase in the vacancy concentrations at temperatures 900 K and 800 K for the As and P doped samples, respectively. These thermally created vacancies were identified as complexes consisting of the vacancy and three donor atoms, the same defects observed earlier in highly doped as-grown material [1]. These defects are likely to be responsible for the electrical deactivation detected at high doping concentrations [1,2]. Their formation can be explained by the kinetic processes observed after annealing the vacancy-donor pairs introduced by the electron irradiation [3]. We have furthermore observed the dissociation of these defects at 1100 K and estimated their formation and dissociation energies. [1] V. Ranki et al., Physical Review B 67, 041201 (2003). [2] P. A. Packan, Science 285, 2079 (1999). [3] V. Ranki et al., Physical Review Letters 88, 105506 (2002).

B/PII.06

IMPACT OF DOPANT PROFILES ON THE END OF RANGE DEFECTS FOR LOW ENERGY GERMANIUM PREAMORPHIZED SILICON

R. A. Camillo-Castillo(a), M. E. Law(a), K. S. Jones(a) and L. M. Rubin(b); (a) SWAMP Center, Department of Materials Science and Engineering, University of Florida, Gainesville FL, U. S. A., (b) Axcelis Technologies. Beverly MA, U. S. A.

As the industry continues to aggressively scale CMOS technology, the shift to lower energy ion implantation becomes essential. The consequent shallower amorphous layers result in dopant profiles that are in closer proximity to the end of range (EOR) damage and therefore a better understanding of the interaction between the dopant atoms and the EOR is required. A study is conducted on the influence of dopant profiles on the behavior of the EOR defects. Czochralski-grown silicon wafers are preamorphized with 1x1015cm-2, 10keV Ge+ ions and subsequently implanted with 1x1015cm-2, 1keV B+ ions. A sequence of rapid thermal and furnace anneals are performed at 750oC under a nitrogen ambient for periods of 1 second up to 6 hours. Plan view transmission electron microscopy (PTEM) reveal a significant difference in the defect evolution for samples with and without boron, suggesting that the boron influences the evolution of the EOR defects. The extended defects observed for samples which contain boron appear as dot-like defects which are unstable and dissolve after very short anneal times. The defect evolution however, in samples without boron follows an Oswald Ripening behavior and form {311}-type defects and dislocation loops. Hall Effect measurements denote a high initial activation and subsequent deactivation of the dopant atoms which is characteristic of the formation of boron interstitial clusters. Diffusion analyses via Secondary Ion Mass Spectroscopy (SIMS) support this theory.

B/PII.07 STUDY OF HIGHLY BORON-DOPED SI/SIGE EPITAXIES BY RTCVD

A. Talbot(a), G. Avenier(a), F. Deleglise(a), C. Fellous(a), G. Vincent(b) and D. Dutartre(a); (a) STMicroelectronics, Crolles, France, (b) UJF, LTM, LETI – DTS, CEA Grenoble, Grenoble, France

As the critical size of MOSFET becomes smaller and smaller and complexity of architectures increases, selective and non-selective depositions of in situ doped film become extremely attractive for the realisation of new devices architectures like, elevated sources/drains in CMOS or extrinsic bases in bipolars. Epitaxial layers were grown in a 200mm industrial single wafer reactor. Firstly, we investigate the boron incorporation in Si/SiGe non selective epitaxy based on SiH4/GeH4/B2H6/H2 chemistry at low temperature (550-750°C). The influence of temperature and germanium content on the boron incorporation is presented. Free carrier density deduced from four probes measurements varied from 8E18 to 2.5E20 holes/cm3 as-deposited. We demonstrate that both the boron incorporation and the film conductivity are improved in SiGe compared to Si. In addition, combining the dose of substitutional boron atoms, deduced from the X-ray diffraction shift, with the resistivity results, we can infer a significant enhancement of the hole mobility in SiGe compared to Si (at least for moderate doping levels around 1E20 h/cm3). In a second part, the high boron-doping of selective Si epitaxy based on SiH2Cl2/B2H6/HCl/H2 chemistry at reduced pressure (<20 Torr) and at low temperature (700-850°C) is examined. Boron incorporation is observed to decrease with increasing HCl flow and the electrical doping level to increase with temperature. We also report a strong increase of the growth rate with the dopant flow (6 times higher for B2H6/DCS=0.01) that will be discussed. Epitaxies that are fully selective against Si3N4 have been demonstrated with free carrier densities as high as 1E20 h/cm3.

B/PII.08 ON THE USE OF DEEP LEVEL TRANSIENT SPECTROSCOPY AND DIFFUSION SIMULATION TO STUDY A PHYSICALS MECHANISMS RELATED TO LOW-ENERGY BORON IMPLANTATION

M. Hanine, J. Marcon and M. Masmoudi, LEMI-University of Rouen, France

This paper describes a qualitative study of the physical mechanisms related to low-energy ion implantation, one of the most promising options towards making ultra shallow p + n junctions. The most current dopant (the only impurity able to serve when there is a high concentration of p-type dopant) used by industries, as well as the most risky (due to its high depth penetration), is boron. It turned out that boron interstitial atoms can diffuse over long distances even at room temperature until they meet trapping sites. As this result is generally neither evidenced by traditional simulators (for ex. Monte-Carlo which predicts a projected range significantly shorter than that of SIMS) nor by SIMS measures (since below 1.1016cm-3 concentrations the SIMS resolution is obtained), we introduce an original approach based on boron concentration profiles according to depth with a simple diffusion activation model in association with Deep Level Transient Spectroscopy (DLTS).

B/PII.09 AN RELIABLE PROCEDURE FOR THE ANALYSIS MULTI-EXPONENTIALS TRANSIENTS THAT ARISE IN DEEP LEVEL TRANSIENT SPECTROSCOPY

M. Hanine, M. Masmoudi and J. Marcon, LEMI-University of Rouen, France

In this paper, a reliable procedure is detailed, which allows a fine as well as robust analysis of the deep defects in semiconductors. In this procedure where capacitance transients are considered as multi-exponential and corrupted with Gaussian noise, our new method of analysis, the LM-DLTS (Levenberg-Marquardt Deep Level Transient Spectroscopy), is associated with two other high-resolution techniques, i. e. the MP-DLTS (Matrix-Pencil Deep Level Transient Spectroscopy) which provides an approximative number of exponential components contained in the capacitance transients and Prony's method recently revised by Osborne in order to set the initial parameters. Finally, when the signal-to-noise ratio is low, and in the aim of getting precise results, a few smoothing algorithms were tested. The wavelet transform denoising was specifically compared using Donoho's universal thresholding algorithm with that of the polynomial fitting with linear least squares. Our findings evidence how the smoothing quality can be controlled under certain conditions while avoiding both the distortions in the shape of the capacitance transients and the DLTS spectras.

B/PII.10 Si SELF-DIFFUSITY USING ISOTOPICALLY PURE 30Si EPITAXIAL LAYERS

S. R. Aid(a), T. Sakaguchi(a), K. Toyonaga(a), Y. Nakabayashi(a), S. Matumoto(a), M. Sakuraba(b), Y. Shimamune(2), Y. Hashiba(b), J. Murota(b), K. Wada(c) and T. Abe(d); (a) Department of Electronics and Electrical Engineering, Keio University, Japan, (b) Research Institute of Electrical Communication, Tohoku University, Japan, (c) Department of Materials Science, MIT, Cambridge MA, U. S. A., (d) Shin-Etsu Handoutai, Isobe, Japan

In order to understand the properties of point defects in Si, it is important to clarify temperature dependence of Si intrinsic self-diffusion coefficients over wide temperature range. In this work, we used highly isotopically enriched 30Si epi-layers as a diffusion source to bulk and epi-layers Si and evaluated self-diffusion. 30Si epi-layers were grown on each CZ-Si substrate and non-doped epi-layer grown on CZ-Si substrate using low pressure CVD with 30SiH4. Diffusion was performed in resistance furnaces under pure Ar(99.9%) atmosphere at temperature between 867C～1300C. After annealing, the concentration of the respective Si isotopes were measured with SIMS. This analysis were performed using CAMECA IMS-4f instrument with 3keV O2+. Diffusion coefficients of 30Si (called Si self-diffusity, DSD) were determined using numerical fitting process with 30Si SIMS profiles. We found no major differences in self-diffusity between in bulk Si and epi-layers Si. It was shown that within 867C～1300C range, DSD can be described by an Arrhenius equation with one single activation enthalpy, DSD = 14exp(-4.37eV/kT). The present result is in good agreement with that of Bracht et. al.

B/PII.11 DETERMINATION OF SILICON SELF-INTERSTITIAL DIFFUSIVITY USING ISOTOPICALLY PURE 30SILICON MULTILAYERS

S. Seto(a), T. Sakaguchi(a), Y. Nakabayashi(a), S. Matsumoto(a), J. Murota (b), K. Wada(c) and T. Abe(d); (a) Department of Electronics and Electrical Engineering, Keio University, Japan, (b) Research institute of Electrical Communication, Tohoku University, Japan, (c) Department of Materials Science and Engineering, MIT, Cambridge MA, U. S. A., (d) Isobe R&D Center, Shin-Etsu Handotai, Japan
Si self-interstitial diffusivities have been investigated using B-doping superlattice. However, the influence of the charge and strain of boron in Si on point defect concentration is unavoidable. To overcome these difficulties, we fabricated the isotopically pure 30Si multilayers and determined directly the Si self-interstitial diffusivity by monitoring the spread of the respective 30Si multilayers after the oxidation of the surface. Samples were prepared with the alternative epitaxial growth of 30Si and natural Si by low temperature gas-source molecular-beam epitaxy on Si(100) substrates (float zone, B doped) using 30SiH4 and normal SiH4, respectively. They consisted of about 500 nm-thick epitaxial layer, containing 30Si spikes of 10 nm width. 30Si profiles were measured by SIMS and Si diffusivities were determined from numerical fitting method. From the reduction of the oxidation enhancement of each 30Si layers with oxidation time, the time-dependence of the concentration of Si self-interstitials from the SiO2/Si interface was confirmed. Finally, Si self-interstitial diffusivities, DI, are obtained: DI=3.48exp(-3.82(eV)/kT). These values are much smaller than Si self-interstitial diffusivities estimated from metal diffusion under several assumptions.

B/PII.12 DIFFUSION MODELS OF BF2+ and B+ IMPLANTED AT LOW ENERGY IN CRYSTALLINE SILICON

L. Ihaddadene-Le Coq, J. Marcon, K. Masmoudi and K. Ketata, Laboratory of Electronic Microtechnology and Instrumentation, University of Rouen, France
An extensive knowledge of the diffusion phenomena occuring in silicon implanted with boron at ulta-low energy is needed to control the junction depth. Secondary ion mass spetrometry has been used to measure dopant profiles in ion implanted samples with ion energy of 500eV (i.e BF2+ 2KeV). Comparison of BF2+ (2 KeV) diffusion profiles and published B+ profiles (500 eV) has been proposed. Using published models (Uematsu), we have investigated and tested a complete simulation program taking into account the BED effect and the fluorine influence. Experimental results have been simulated and consistent parameters have been found to fit the data. Model parameter extractions have been discussed.

B/PII.13 A KINETIC MONTE CARLO ANNEALING ASSESSMENT OF THE DOMINANT FEATURES FROM IMPLANT SIMULATIONS

I. Martin-Bragado, M. Jaraiz, P. Castrillo, R. Pinacho, J. E. Rubio and J. Barbolla, Dpt. of Electronics, University of Valladolid, Spain
Ion implantation and subsequent annealing are essential stages in today's advanced CMOS processing. Although the dopant implanted profile can be accurately predicted by analytical fits calibrated with SIMS profiles, the damage has to be estimated with a MC implant simulator. Some models have been proposed, like the "+n" among others, in an attempt to simplify the anneal simulation. We have used the atomistic kinetic Monte Carlo DADOS to elucidate which are the implant modeling features most relevant in the simulation of transient enhanced diffusion (TED). For the cases studied we find that (i) the spatial correlation of the I,V Frenkel pairs is not critical. (ii) The I and V distributions are shifted by a few Amstrongs with respect to each other. However, there is also a slight difference in shape which is essential to get the correct I-supersaturation. (iii) Quick and noisy MC implant I,V distributions can be directly used (or after smoothing them out) as they can still yield to accurate annealing simulations. (iv) When there is an impurity concentration comparable to the net I-V excess, the full I and V profiles have to be used in order to correctly reproduce the impurity clustering/deactivation.

B/PII.14 ENHANCED OUT-DIFFUSION OF DOPAND DURING VACUUM RAPID THERMAL ANNEALING OF ION-IMPLANTED Si

V. A. Kagadei(a), and A. B. Markov(b); (a) Research Institute of Semiconductor Devices, Tomsk, Russia, (b) Institute of High Current Electronics, Tomsk, Russia
Ultra-shallow ion-implanted layers of Si are necessary to produce modern integral circuits. In order to form ultra-shallow junctions or, in other words, to decrease a dopant diffusion into the bulk of Si during annealing the method of vacuum rapid thermal annealing in condition of dopant transient enhanced out-diffusion was suggested. The transient enhanced out-diffusion of dopand from ion-implanted layer decelerates its diffusion into the bulk of Si. The model of phosphorous diffusion in ion-implanted Si at vacuum rapid thermal annealing in condition of the transient enhanced out-diffusion has been developed in the paper. The model takes into account the influence of non-equilibrium point defects on dopant transient enhanced diffusion as well as out-diffusion. Influence of non-equilibrium defects surface annihilation on phosphorous out-diffusion rate, as well as phosphorous out-diffusion kinetics has been considered. Analysis of calculated data and their comparison with experimental results on rapid thermal e-beam annealing of P-implanted Si is presented. Promising use of vacuum rapid thermal annealing in condition of transient enhanced out-diffusion to form the ultra-shallow junctions is discussed.

B/PII.15 ARSENIC DIFFUSION IN Si AND Si1-XGeX ALLOYS AT 1000°C

S. Uppal(a), J. M. Bonar(b), A. F. W. Willoughby(a) and J. Zhang(c); (a) Materials Research Group, School of Engineering Sciences, University of Southampton, U. K., (b) School of Electronics and Computer Science, University of Southampton, U. K., (c) Department of Electrical Engineering, Imperial College, London, U. K.
Results of Arsenic diffusion under intrinsic diffusion conditions in Si and SiGe (5, 10%) alloys are presented. Epitaxial Si and compressively strained SiGe structures with buried marker layers of arsenic were grown using Molecular Beam Epitaxy. The concentration profiles before and after Rapid Thermal Annealing at 1000 C have been measured using SIMS. An enhancement of As diffusivity in $Si_{0.9}Ge_{0.1}$ compared to Si is observed in agreement with literature. However for As in $Si_{0.95}Ge_{0.05}$ strain seems to compensate the effect of enhancement due to Ge chemical effect. Studies at other temperatures are underway.

B/PII.16 EXCIMER LASER ANNEALING OF SHALLOW As AND B DOPED LAYERS

E. V. Monakhov(a), B. G. Svensson(a), M. K. Linnarsson(b), A. La Magna(c), V. Privitera(c), M. Camalleri(d), G. Fortunato(e) and L. Mariucci(e); (a) Department of Physics, Physical Electronics, University of Oslo, Norway, (b) Solid State Electronics, Royal Institute of Technology, Stockholm, Sweden, (c) CNR-IMM, Catania, Italy, (d) STMicroelectronics, Catania, Italy, (e) CNR-IFN, Roma, Italy
Excimer laser annealing (ELA) of As, B and BF2 implanted Si has been studied by secondary ion mass spectrometry (SIMS), spreading resistance probe (SRP) and transmission electron microscopy (TEM). The implantations have been performed in the energy range from 1 keV to 30 keV with doses of 1e15-1e16 cm-2. ELA has been carried out with the energy densities in the range of 600-1200 mJ/cm2 and the number of laser pulses from 1 to 10. It is shown that ELA results in a more uniform dopant distribution over the doped region with a more abrupt profile edge as compared to those after rapid thermal annealing (RTA). Besides, in contrast to RTA, ELA demonstrates a highly confined annealing effect, where the distribution of dopants in deeper

regions is not affected. SRP measurements demonstrate almost complete activation of the implanted dopants after ELA, and TEM does not reveal extended defects in the ELA treated samples. The depth of the doped layers, abruptness of the profiles and the total doping dose as a function of ELA energy density and number of laser pulses are investigated. Computer simulations of ELA show a good agreement with the experimental data.

B/PII.17 FLASH LAMP PROCESSING FOR BORON IMPLANTED ULTRA SHALLOW JUNCTIONS

W. Skorupa(a), W. Anwand(a), T. Gebel(b) and R. A. Yankov(b); (a) Institute of Ion Beam Physics and Materials Research, Forschungszentrum Rossendorf, Dresden, Germany, (b) Nanoparc GmbH, Dresden, Germany

The successful use of energy pulses from flash lamps for the advanced thermal processing of semiconductors and other materials is of growing interest. For ultra-shallow junction formation in silicon Flash Lamp Processing has become one of the challenging methods to meet the requirements for the next technology nodes defined by the ITRS roadmap. Low energy boron implants have been heat-treated in this way using peak temperatures in the range of 1100°C to 1300°C and effective anneal times down to 2.5 msec. Secondary ion mass spectrometry and four point probe measurements were used to determine the junction depth and the sheet resistance, respectively. Optimum processing conditions using a pulse time of 2.5 msec have been identified, under which one can obtain combinations of junction depth and sheet resistance values that meet the 90 nm and even the 70 nm technology node requirements.

B/PII.18 A SIMPLE TWO-STEP PHOSPHORUS DOPING PROCESS FOR SHALLOW JUNCTIONS BY APPLYING A CONTROLLED ADSORPTION AND A DIFFUSION IN AN OXIDISING AMBIENT

B. Kalkofen, M. Lisker and E. P. Burte, Institute of Micro and Sensor Systems, Otto-von-Guericke-University, Magdeburg, Germany

A simple phosphorus doping technique for shallow junctions will be presented. The low pressure doping process was carried out in a single RTP reactor chamber by using a two step process: a controlled adsorption of phosphorus on the silicon surface and a rapid thermal diffusion in an oxidising ambient without the deposition of an oxide capping layer. A low concentration of 50 vpm phosphine diluted in hydrogen allowed a sufficient and uniform phosphorus supply while the deposition of phosphorus on the reactor walls was insignificant. The phosphine decomposed on the clean silicon surface at a temperature of 550 °C at which the silicon surface is saturated by the adsorbed phosphorus. This ensures an easy control of the exposure step. The shallow junctions were defined by a succeeding rapid thermal annealing at temperatures above the adsorbtion temperature. An oxygen pressure of 20 mbar during the annealing sufficiently prevented the phosphorus from desorption. Therefore, a deposition of an additional oxide-capping layer was not necessary, allowing a more simple processing. This doping methode provides shallow junctions of depths below 50 nm with low sheet resistances below 2 kOhms/sq.

B/PII.19 CHARGE TRANSFER DOPING FOR ULTRA-SHALLOW SOURCE/DRAIN EXTENSION

K. Kimoto(a), T. Tada(b) and T. Kanayama(b); (a) MIRAI-ASET and (b) MIRAI-ASRC, AIST, Tsukuba, Japan

As a novel formation technique of ultra-shallow source/drain extensions (SDE), here we propose the use of charge transfer doping; i.e., when adequate impurities with either a low ionization potential or a high electron affinity are placed near a Si surface, charge transfer occurs between them thereby forming carriers below the surface. We investigated how well this principle works by device simulations and sheet resistance Rs measurements. According to our calculations, Rs of inversion layers induced by surface charges cannot be lowered than a minimum, e.g., 2.1 k ohm/sq. for electrons at a substrate concentration of 1E16cm-3 because carrier generation competes with mobility degradation. In the experiments using Cs ions as positive charges, Rs actually saturated at 3 k ohm/sq. with a sheet carrier density of 1.1-2.7E13cm-2. Thus the Charge Transfer doped SDE (CTE) is ultra-shallow but relatively high in Rs. Drive current Ion was simulated for nMOSFETs with CTE (CTE-MOS) and conventional nMOSFETs (conv.MOS) of 45nm node (tox=0.65nm, Vdd=0.6V) taking into account the short channel effect in such a way that the gate length Lg variation was assumed to be 20% around 18nm and the uniform channel concentration Cc was determined so that Ioff=3.0uA/um at Lg=18nm-20% and then Ion was compared at Lg=18nm+20%. CTE-MOS was found to exceed conv.MOS by 1.4 times in Ion because its Vth shift due to the Lg variation is 1/2.6 and Cc is reduced to 1/3.4 compared to conv.MOS.

B/PII.20 SHALLOW TRENCH ISOLATION DIMENSIONS EFFECTS ON LEAKAGE CURRENT AND DOPING CONCENTRATION OF ADVANCED p-n JUNCTION DIODES

A. Poyai(a), I. Rittaporn(a), E. Simoen(b), R. Rooyackers(b) and C. Claeys(b,c); (a) TMEC, Chachoengsao, Thailand, (b) IMEC, Leuven, Belgium, (c) E. E. Dept., KU Leuven, Belgium

The down-scaling of CMOS technology necessitates the implementation of advanced isolation schemes. Shallow trench isolation (STI) is the only viable approach for technologies with sub 0.25 m feature size. On the other hand, reducing the p-n junction dimensions puts more and more emphasis on peripheral and corner effects. This paper investigates the impact of STI dimensions on leakage current and doping concentration of different geometry n+-p-well junctions compatible with submicron CMOS technology processed on 200 mm p-type substrates. From the current-voltage (I-V) and capacitance-voltage (C-V) characteristics, a higher leakage current and p-well doping concentration was found for the smaller active area with the wider STI. As will be discussed for these effects, the stress from the upper and lower trench's corners should be taken into account.

B/PII.21 SOLID PHASE EPITAXIALLY ACTIVATED ANTIMONY ION-IMPLANTED SILICON N+/P JUNCTION FOR SUB-100 nm METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICES WITH EMERGING OF HIGH-K DIELECTRICS

S. G. Tavakoli, S. Baek, and H. Hwang, Department of Materials Science and Engineering, Kwang-Ju Institute of Science and Technology, Republic of Korea

Shallow, low-resistive n+/p junction was investigated for sub 100-nm advance metal-oxide-semiconductor-field-effect-transistors (MOSFETs) using antimony and arsenic ion-implantation and low temperature rapid thermal annealing -increased gate leakage current due to high-permittivity gate dielectric crystallization during high temperature source and drain dopant activation imposes low temperature annealing for next generation devices-. In contrast to arsenic implanted junctions, Sb-doped specimens showed shallower junction depth, lower sheet resistance and leakage current at low temperature processing (600 C). In addition, Ge pre-amorphization prior to As-implant was used to fully amorphize Si for ideal solid-phase regrowth. Pre-amaorphized As-doped samples did not result in highly activated junctions at low temperature. The results indicated the superiority of antimony to arsenic as a dopant for ultra-shallow and low resistive source and drain extensions. Arsenic will not be a proper candidate because of higher sheet resistance -as a consequence of presence of inactive As-vacancy clusters- and

higher leakage current for devices that should be fabricated at low temperature with implementing of high-k dielectric-metal electrode gate stack in next generation MOSFETs.

B/PII.22 LOW TEMPERATURE SOLID PHASE EPITAXIALLY ACTIVATED, SHALLOW p+/n Ga DIRECT ION-IMPLANTED JUNCTION FOR SUb-100 nm TECHNOLOGY NODE

S. G. Tavakoli, K. Lee, S. Baek and H. Hwang, Department of Materials Science and Engineering, Kwang-Ju Institute of Science and Technology, Republic of Korea

High diffusivity of Ga in SiO2 prevented the use of Ga (with SiO2 as a mask) in conventional device fabrication. Focused ion beam implantation has been used to overcome this problem. However, increased gate leakage current due to high-permittivity gate dielectric crystallization during high temperature source and drain dopant activation imposes low temperature annealing for next generation devices. This issue proposes the possibility of Ga as a proper dopant with direct ion-implantation in next generation of metal-oxide-semiconductor-field-effect-transistor applications. Shallow p+ /n junction was fabricated with low energy Ga+ ion-implantation and low temperature annealing. Junctions had good electrical characteristics at low implantation energy and appropriate implantation dose. Gallium implanted junctions regrew solid phase epitaxially at low thermal budget (at 600 ºC for 1 min). It resulted in abnormal Ga+ activation and a low leakage current density. The results are comparable to the previously reported BF2+ implanted junctions which require a long annealing time at this low temperature. Consequently, Ga can be a proper candidate as a p-type dopant for ultra-shallow junction fabricated with direct ion-implantation and low temperature annealing for high-k gate dielectric MOSFET applications.

B/PII.23 BEHAVIOUR OF LOW ENERGY AS IONS IMPLANTED IN SI THROUGH A THIN OXIDE LAYER

M. Ferri(a), A. Parisini(a), S. Solmi(a), M. Bersani(b), D. Giubertoni(b) and M. Barozzi(b); (a) CNR-IMM Bologna, Italy, (b) ITC-irst, Povo, Italy

The diffusion and the annealing mechanisms of the low energy As implanted Si have been investigated by comparing Secondary Ion Mass Spectrometry (SIMS) and simulated profiles. Z-contrast scanning transmission electron microscopy (STEM) imaging has been also used to determine the As local distribution at the sample surface. The implantation has been performed through a thermally grown 11 nm thick oxide, with energies of 3, 5 and 10 keV at a dose of 7x1014 cm-2 and it has been followed by isothermal annealing with a rapid thermal system in the range 800-1000°C in nitrogen atmosphere. Arsenic implanted samples at energy of 5 keV and doses of 7x1014 and 1x1015 cm-2 without oxide mask have been also prepared and annealed in the same conditions. SIMS and STEM profiles show an As pile-up in the first 3-5 nm of the Si matrix in proximity of the SiO2/Si interface that gives rise to a drastic reduction of dopant able to diffuse deep in the bulk. The As diffusivity in the Si region in proximity of the surface is strongly reduced. This phenomenon is more evident at the lowest implantation energy, and it is present also in the samples without pre-oxidation. However, beyond this surface region, the As profiles show a moderate transient enhanced diffusion (TED) during the first steps of annealing which increases with reducing temperature. The phenomenon has been evaluated and discussed.

B/PII.24 STUDIES OF ULTRA-SHALLOW N+ P JUNCTION CHARACTERISTICS FORMED BY LOW- ENERGY AS-IMPLANTATION

D. Girginoudi(a), N. Georgoulas(a), A. Thanailakis(a) and E. K Polychroniadis(b); (a) Department of Electrical and Computer Engineering, Democritus University of Thrace, Xanthi, Greece, (b) Physics Department, Aristotle University of Thessaloniki Greece

Currently, shallow junction scaling is achieved by reducing the implant energy and the thermal budget of the rapid thermal annealing (RTA) cycle. The reduced RTA cycle decreases the transient enhanced diffusion (TED) of dopants, but this may lead to a degradation of the electrical junction quality due to low dopant electrical activation and incomplete defect annealing. Low energy implantation of As, at doses above 5·1014cm-3, induces amorphisation in the implanted layer, generating end-of-range defects beyond the amorphous-crystalline interface during annealing. As the implant energy is decreased, the distance between the junction depth and the depth at which these defects are located becomes smaller and, therefore, the electrical characteristics of junctions will be easily affected by the residual defects. Furthermore, the processes occurring at the surface during RTA (out-diffusion and segregation of dopants) is expected to affect the TED and the electrical activation. The purpose of this work is to investigate the advantages and disadvantages of reducing the energy of As ion implantation by measuring the characteristics of the fabricated n+-p junctions. The implantation conditions were: energy from 15 to 2 keV with high dose of 1·1015 cm-2, and the RTA conditions were: temperature 650 ºC £ T £ 950 ºC and time t = 10 and 20 sec. A two-step annealing (650 ºC/10s + 950 ºC/10s) was adopted, in order to minimize TED effects. TEM studies were performed in order to investigate the defect formation and dissolution, as well as SIMS, sheet resistance and differential Hall effect measurements to study both the dopant diffusion and electrical activation, and the detailed results obtained will be presented and discussed.

B/PII.25 HIGH RESOLUTION ELASTIC RECOIL DETECTION ANALYSIS OF ULTRA SHALLOW IMPLANTS

G. Dollinger(a), A. Bergmaier(a), J. Fruehauf(a), L. Goergens(a), F. Koch(a), P. Neumaier(a), W. Vandervorst(b), J. Schulze(c) and I. Eisele(c); (a) Physik Department, Technische Universitaet Muenchen, Garching, Germany, (b) IMEC, Leuven, Belgium, (c) Universitaet der Bundeswehr, Neubiberg, Germany

Implantation of dopants with ion energies around 1 keV or lower are commonly investigated in order to generate ultra shallow junctions in silicon. Understanding the electrical properties requires a detailed knowledge of the implantation profile and the dopant distribution after heat treatment processes. Since the commonly used SIMS profiling generates artifacts at interfaces and close to the surface we employed high resolution elastic recoil detection (ERD) analysis using swift heavy ion beams for quantitative elemental profiling with a depth resolution of about 0.5 nm close to the surface. We show profiles of 500 eV boron implants through ultra thin SiO2- and SiON-layers before and after heat treatment. They show clear enhancement of boron close to the oxide-silicon interface after heat treatment which increases with nitrogen content. There is evidence that this enhancement is electrical active and contributes to the overall conductance of the junction. A second set of data is presented for delta-doped silicon which was obtained by MBE overgrowth of sqr(3) x sqr(3) reconstructed boron surface phases with amorphous silicon and subsequent annealing at various temperatures. At 700°C a main portion of the boron remains at the delta-position. However, high resolution ERD-channeling does not show any significant substitutional configuration while at higher annealing temperature the boron diffuses away from the original position.

B/PII.26 NON-UNIFORM DEPTH PROFILE OF THE SITE LOCATION OF AS IMPLANTED IN Si AT ULTRA-LOW ENERGIES

S. Milita(a), F. D'Acapito(b), M. Servidori(a), M. Malvestuto(c) and F. Boscherini(c); (a) CNR IMM Bologna, Bologna, Italy, (b) INFM-OGG c/o E. S. R. F. Grenoble, France, (c) INFM and Dipartimento di Fisica, Università di Bologna, Italy

In this study we intend to give a contribution to the structural investigation of defects in very shallow junctions typical of miniaturized electronic devices. Silicon wafers implanted with As ions at 5 keV and fluence of $1*10^{15}$ As/cm^2 were treated by rapid thermal annealing or spike annealing. The lattice location of the As atoms has been determined by Extended X-ray Absorption Fine Structure (EXAFS) in total reflection mode with a beam energy corresponding to the As K absorption edge. The measurements were carried out at the GILDA beamline of the European Synchrotron Radiation Facility. For incidence angles (α) greater than the critical angle (α_c) of total reflection, the beam penetration in the sample is about 150 nm, so that the whole implanted layer was probed. By contrast, for $\alpha < \alpha_c$ the beam is confined within the first 8 nm and only the shallower part of the implanted As was then analyzed.. The comparison between the two data sets revealed marked differences corresponding to different sites for As along the implantation profile. The analysis of the whole layer evidenced that, thanks to the appreciable signals from up to the third coordination shell, As is coordinated on average to 3 Si atoms with a distance of 0.241 nm. This is close to the configuration found in low density As in Si, though the local disorder appears to be higher in our samples. The analysis of the shallower part of the implant evidenced an As-Si coordination distance of 0.237 nm together with an As-As coordination distance of $\approx$0.258 nm. This finding is in agreement with literature data on high density As in Si and well evidences the non uniformity of the As occupation sites which characterizes the very shallow implant profiles.

B/PII.27

FUNDAMENTAL CHARACTERIZATION AND MODELING OF THE EFFECT OF DIFFERENT NITRIDE SIDEWALL SPACER PROCESSES ON BORON DOSE LOSS IN ULTRA-SHALLOW JUNCTION FORMATION

P. Kohli(a,b), S. Chakravarthi(b), A. Jain(b), H. Bu(b), M. Mehrotra(b), S. T. Dunham(c) and S. K. Banerjee(a); (a) The University of Texas Austin, U. S. A., (b) Texas Instruments, (c) The University of Washington at Seattle, U. S. A.

A nitride spacer with an underlying deposited TEOS oxide, that behaves as a convenient etch stop layer, is a popular choice for sidewall spacer in modern CMOS process flows. In this work we have investigated the effect of the silicon nitride spacer process chemistry on the boron profile in silicon and the related dose loss of B from Si into silicon dioxide. This is reflected as a dramatic change in the junction depth, junction abruptness and junction peak concentration for the different nitride chemistries. We find that the silicon nitride influences the concentration of hydrogen in the silicon dioxide and the different nitride chemistries result in different concentrations of hydrogen in the silicon dioxide during the final source/drain anneal. The presence of H enhances the diffusivity of B in the silicon dioxide and thereby results in a significant dose loss from the Si into the silicon dioxide. In this work we show that this dose loss can be minimized and the junction profile engineered by choosing the desirable nitride chemistry.

Friday, May 28, 2004 Morning

Session VI: Silicon processing III
Session chair: S. Cristoloveanu (CNRS-ENSERG, France)

B-IX.1 08:30 -Invited-

CRITICAL DOPING REQUIREMENTS FOR SDE APPLICATIONS IN </= 65 nm DEVICE MANUFACTURING

S. Mehta, U. Jeong and J. Liu, Varian Semiconductor Equipment Associates, Gloucester MA, U. S. A.

Ion implantation has long been considered as a commodity in semiconductor device manufacturing. Historically, precision of beam incident angle was not a critical requirement. However, with the miniaturization of semiconductor devices, the traditional tolerance to errors in beam incident angle are becoming less acceptable. This places significant constraints on the ability of implanters to meet the precision requirements of dopant placement necessary to sustain device performance. In this paper we will discuss the effect of beam incident angle in SDE applications traditionally performed on high current implanters. Device parametric performance was investigated using TCAD simulations. With implant energies for SDE reaching sub keV levels, these implants are typically performed in decel mode. Depending on the design of the implanter, use of decel mode can introduce a finite amount of energy contamination. Effects of this energy contamination on device performance was also investigated using TCAD simulations.

B-IX.2 09:10

DOPANT INDUCED DAMAGE IN SILICON AFTER LOW ENERGY ION IMPLANTATION STUDIED BY COMBINED X-RAY SCATTERING TECHNIQUES

L. Capello(a), T. H. Metzger(a) and M. Servidori(b); (a) E. S. R. F., Grenoble, France, (b) CNR-IMM Bologna, Italy

Low energy ion implantation might become the solution to fabricate ultra shallow junctions for the next generation of CMOS devices. The unavoidable defects present after implantation play a crucial role for the device performance. The structural evolution of post implantation defects needs to be characterised on an atomic level. It will be demonstrated that the combination of several x-ray scattering methods represents an ideal tool to achieve this task: x-ray diffraction reveals the depth resolved strain profile and specular reflectivity gives the complementary density profile. Grazing incidence diffuse x-ray scattering (GI-DXS) is used to determine, with depth resolution, whether the defects are point-like defects or of extended nature. For the use of GI-DXS the high brilliance of synchrotron radiation of the ESRF is mandatory. Si (001) wafers were implanted with As and BF2 at 3keV and annealed at various thermal budgets. Extrinsic stacking fault formation is observed in both systems. We found dopant segregation underneath SiO2/Si interface and studied the slow solid phase epitaxial regrowth at low temperatures (between 5000C and 7000C). This research is supported in the framework of the European Project IMPULSE (ion IMPlantation at Ultra-Low energy for future SEmiconductor devices).

B-IX.3 09:30

ATOMISTIC MODELING OF DEFECT EVOLUTION IN Si FOR AMORPHIZING AND SUBAMORPHIZING IMPLANTS

P. Lopez, L. Pelaz, L. A. Marques, I. Santos, M. Aboy and J. Barbolla Department of Electronics, University of Valladolid, Spain

Preamphization followed by low temperature solid phase epitaxial regrowth have been probed to provide excellent results for the formation of ultra shallow junctions with low resistivity. Therefore, predictive simulators which include amorphization and regrowth models in Si are demanded. We have developed an atomistic model that encompasses different damage configurations, ranging form point defects to more complex agglomerates, including amorphous pockets and continuous amorphous layers. The model takes into account dynamic anneal during the implant and the different shapes and sizes of amorphous pockets and other defect structures. Thus, it captures the critical dependence of damage accumulation on implant parameters (dose, dose-rate, ion mass, target temperature) and the characteristic annealing behaviour of different damage structures. The same model can be consistently applied to sub-amorphizing and amorphizing implants. The model predicts the formation of continuous amorphous layers and the residual defects, which influence dopant diffusion and activation. In subamorphizing implants, amorphous pockets are not connected, and after their regrowth they leave behind the local excess of atoms. When a continuous amorphous layer is formed and extends to the surface, the excess or deficit atoms contained within the layer are swept to the surface as regrowth takes place, and only the defects beyond the amorphous/crystalline interface remains.

B-IX.4 09:50

LATTICE STRAIN INDUCED BY BORON-INTERSTITIAL CLUSTERS IN CRYSTALLINE SILICON

G. Bisognin(a), D. De Salvador(a), E. Napolitani(a), L. Aldegheri(a), A. V. Drigo(a), M. Berti(a), A. Carnera(a), S. Mirabella(b), E. Bruno(b), G. Impellizzeri(b) and F. Priolo(b); (a) INFM and Dipartimento di Fisica, Università di Padova, Italy, (b) MATIS - INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Italy

The nature of the boron interstitial-clusters (BICs), small, immobile and electrically inactive defects present after B implantation and annealing in crystalline Si, is nowadays not well clear. To study the composition and the lattice strain induced by BICs, a narrow, high-concentration B box sandwiched between a 200nm Si cap and an array of B delta-doping (d) was grown by molecular beam epitaxy. The cap was implanted with 20 keV Si at two different doses (0.5 and 1 x 10^14 at/cm2) to provide the source of self-interstitials (I's) and then annealed to form BICs. The samples were further annealed to dissolve BICs. The B chemical profiles of the box and of the d-array were measured by means of secondary ion mass spectrometry, and then analysed in order to quantify the amount of B and of I's trapped at the BICs. The BIC composition with a B to I ratio ~(3:1) was found to be independent of Si implantation dose. Using high resolution x-ray diffraction (HRXRD), we quantified the lattice strain in the B box containing the BICs. An accurate analysis of the gap fringes in the HRXRD patterns demonstrates that a strong compressive strain is present in the B box as a consequence of BICs formation. The strain integral is proportional to the B dose contained in the BICs. The

determination of this proportionality constant provides a quantitative description of the average lattice deformation induced by BICs and allows an experimental test of theoretical models for BICs atomic structures.

B-IX.5 10:10

DIFFUSE X-RAY SCATTERING AND RUTHERFORD BACKSCATTERING RESPONSES TO SMALL SELF-INTERSTITIAL CLUSTERS IN SELF-ION IRRADIATED SI

S. Milita(a), V. Mocella(b), M. Servidori(a), G. Lulli(a), E. Albertazzi(a), M. Bianconi(a), A. Satta(c), S. Balboni(d) and L. Colombo(c); (a) CNR IMM Bologna, Italy, (b) Sezione di Napoli, Italy, (c) INFM and Dipartimento di Fisica, Università di Cagliari, Italy, (d) CeSIA-Settori Reti e Comunicazioni, Università di Bologna, Italy

The analysis of the Diffuse X-ray Scattering (DXS) is an extremely powerful and non-destructive tool to investigate the point or extended defects introduced in crystals by ion implant. In this study we investigate the capability of DXS to identify the atomic structure of simple defects in silicon. In previous works, the same problem was investigated from the point of view of the Rutherford backscattering ion-channelling (RBS-C) technique. In that case, an atomistic model of lightly damaged Si lattice was obtained by inserting a distribution of self-interstitial defects in a supercell with size of the order of 10^6 atoms. The system was then structurally relaxed by the application of the classical EDIP potential. The comparison of simulated and experimental RBS-C measurements, showed that different models, either of elementary interstitials (the split <110>) or of small (2 and 4 interstitials) clusters, can reproduce, within the uncertainty of the procedure, spectra measured under different alignment conditions in a sample implanted with 180 keV, 10^{14} Si^+/cm^2 ions. Numerical calculations of DXS patterns generated by each of these defects have been carried out close to several reciprocal lattice points (RELPs). The diffuse scattering amplitude, obtained in kinematical approximation, is given by the difference between the amplitude scattered by deformed crystal and that scattered by the perfect one. The qualitative analysis of the intensity distributions around selected RELPs suggests that using DXS it is possible to discriminate among the different self-interstitial defects compatible with the RBS-C results.

10:30 **BREAK**

Session X: Defects in silicon
Session chair: M. Bersani (ITC-irst, Italy)

B-X.1 10:50 -Invited-

MODELING OF EXTRINSIC DEFECT EVOLUTION IN ION IMPLANTED SILICON UPON THERMAL ANNEALING

C. J. Ortiz(a), B. Colombeau(b), F. Cristiano(c), A. Claverie(c) and N. E. B. Cowern(b); (a) Fraunhofer IISB, Erlangen, Germany, (b) University of Surrey, Guildford, U. K., (c) Pole Implantation Ionique CEMES/LAAS-CNRS, Toulouse, France

In the fabrication of transistors, ion implantation is nowadays the most common and accurate way to introduce dopants in silicon. However, collisions of incident ions with host atoms generate a high concentration of vacancies and self-interstitials. During following thermal annealings, these latter can either recombine with vacancies, diffuse toward the surface and recombine, or agglomerate to form extrinsic defects. Depending on the thermal annealing and initial self-interstitial supersaturation, these defects can adopt different geometries and/or sizes but they always maintain in all cases a self-interstitial supersaturation in their vicinity. This supersaturation is responsible for the so-called transient enhanced diffusion (TED) of dopants, detrimental for the fabrication of ultra-shallow junctions that are required in transistors of next generations. Therefore, it is mandatory to properly predict the nucleation and evolution of such defects. After a short introduction on different types of defects that can be found in ion implanted silicon, we will present the physically based model we developed to predict the evolution of extended defects. The kinetic model we propose is implemented one-dimensionally and accounts for the nucleation, growth and dissolution of small self-interstitial clusters up to {113} defects during thermal annealing. Then, we will show how a consistent set of physical parameters can be extracted by means of a genetic algorithm from self-interstitial supersaturation and TEM measurements. Finally, the ability of this calibrated model to predict depth and size distributions of extended defects as well as the self-interstitial supersaturation evolution under a wide range of experimental conditions will be demonstrated.

B-X.2 11:30

FLUORINE INFLUENCE ON POINT DEFECT DENSITY IN PREAMORPHIZED SILICON

G. Impellizzeri(a), J. H. R. dos Santos(a), S. Mirabella(a), F. Priolo(a), E. Napolitani(b) and A. Carnera(b); (a) INFM-MATIS and Dipartimento di Fisica e Astronomia, Università di Catania, Italy, (b) INFM and Dipartimento di Fisica, Università di Padova, Italy

We investigated the fluorine interaction with Si self-interstitials (Is) in preamorphized Si by means of molecular beam epitaxy (MBE) grown B- or Sb- spikes, used as sensitive markers of Is or vacancy concentration, respectively. F was implanted at different energies and doses into preamorphized Si, that was subsequently recrystallized by solid phase epitaxy. This procedure causes the formation, beyond the original amorphous-crystalline interface, of the end of range (EOR) defects which, by further thermal annealing, release Is provoking the well-known boron transient enhanced diffusion (TED). Our results show that the F presence strongly reduces the boron TED up to its complete suppression, while, at the same time, F induces an increase of the Sb diffusion. Moreover, no B-F chemical bonding occurs, while F clearly reduces Is density, causing the boron TED reduction and the Sb enhanced diffusion. Besides, after thermal anneals, F atoms diffuse towards the surface and the bulk, and partially accumulate at the EOR region. F completely leaves the sample only after 1100°C annealing treatments, and, in this condition, no significant boron TED reduction is observed. In addition, we report that F is able to reduce the boron diffusion also under equilibrium condition. In conclusion, we have shown a clear interaction between F and point defects in Si which strongly influences the B or Sb diffusion in Si, both under equilibrium and non-equilibrium conditions.

B-X.3 11:50

THE ROLE OF SILICON INTERSITIALS IN THE DEACTIVATION AND REACTIVATION OF HIGH CONCENTRATION B PROFILES

M. Aboy(a), L. Pelaz(a), L. A. Marqués(a), J. Barbolla(a), V. C. Venezia(b), R. Duffy(b) and P. B. Griffin(c); (a) University of Valladolid, Spain, (b) Philips Research Leuven, Belgium, (c) Stanford University, U. S. A.

Boron implantation into preamorphized Si, followed by low temperature solid phase epitaxial regrowth (SPER), has gained considerable interest as it produces high activation with low diffusion, thereby creating shallow and abrupt junctions. However, in the presence of high B concentrations, the activation achieved during SPER hardly exceeds a threshold concentration in the order of 3x1020 cm-3, and moreover, deactivation occurs during additional annealing. Kinetic Monte Carlo atomistic simulations are used to investigate the physical mechanisms for B cluster formation and dissolution at high B concentrations, and the role of Si interstitials in these processes. We have shown that B clustering in crystalline Si follows a high interstitial content path, and B clusters are formed even for relatively low B doses. However, when the B profile does not overlap with the end of range defects from a preamorphizing implant, the deactivation mechanism depends strongly on the B concentration. B clustering only occurs for B concentrations above 3x1020 cm-3. We have studied the role of the Si interstitials injected from the end of range damage in B deactivation and also in the phenomenon of uphill diffusion. B cluster dissolution follows a low interstitial content path in all cases. This is compatible with B cluster stabilization in the presence of excess Si interstitials, observed in oxidation experiments.

B-X.4 12:10

THE INTERACTION BETWEEN XE AND F IN SI (100) PRE-AMORPHISED WITH 40 KEV XE AND IMPLANTED WITH LOW ENERGY BF2

M. Werner(a), J. A. van den Berg(a), D. G. Armour(a), G. Carter(a), T. Feudel(b), M. Herden(b), M. Bersani(c), D. Giubertoni(c), P. Bailey(d) and T. C. Q. Noakes(d); (a) Joule Physics Laboratory, Institute of Materials Research, University of Salford, U. K., (b) AMD Saxony, Dresden, Germany, (c) ITC IRST, Povo Italy, (d) CCLRC Daresbury Laboratory, Daresbury, U. K.

The pre-amorphisation of Si by Xe ions of energies of up to several tens of keV before source/drain extension type implants, is an attractive alternative to Ge or Si, for reasons of producing sharper amorphous/crystalline interfaces and reduced floating body effects in SOI structures. However upon annealing implanted Xe appears to interact with F originating from the BF2 implant. BF2 was implanted at energies of 1 and 3 keV to doses of 7 E14 cm-2 into crystalline Si(100) samples and samples implanted with 40 keV Xe ions to a dose

yielding an amorphised layer of approximately 35 nm depth. They were subsequently annealed over a range of temperatures ranging from 600°C to 1130°C, and times, using processes that included rapid thermal (RTA), spike and furnace annealing. Samples were investigated by medium energy ion scattering (MEIS), using 100 keV He+ ions, secondary ion mass spectrometry (SIMS) and X-ray photo-electron spectroscopy (XPS). MEIS studies showed that upon of any of the annealing steps, most if not all implanted Xe accumulated at depths of 7 nm for the 1 keV and 13 nm for the 3 keV implant. This equates to approximately 3 times the depth of the mean projected range (Rp) of both the B and the F from the BF2 implant, rather than diffuse out to the surface. SIMS showed that in the pre-amorphised samples, between 6 - 9 % of the implanted F migrates into the bulk and is trapped at this depth in a ~ 1:1 ratio to Xe. A small fraction of the implanted B is also trapped. The effect is interpreted in terms of the formation of a damage structure within the amorphised Si, which leads to a F stabilised Xe bubble or XeF compound formation.

B-X.5 12:30

ROOM TEMPERATURE MIGRATION OF SUBSTITUTIONAL BORON IN SILICON BY KICK-OUT MECHANISM

E. Napolitani(a), D. De Salvador(a), A. Carnera(a), S. Mirabella(b) and F. Priolo(b); (a) INFM and Dipartimento di Fisica, Università di Padova, Italy, (b) MATIS - INFM and Dipartimento di Fisica e Astronomia, Università di Catania, Italy

In this paper we provide an experimental evidence of the long-range migration of substitutional boron in silicon at room temperature (RT) through its interaction with migrating self interstitials (I's), i.e. via the kick-out mechanism. Silicon samples grown by Molecular Beam Epitaxy with substitutional B deltas were depth profiled by Secondary Ion Mass Spectrometry (SIMS) using O2+ ions. The measurements were done on crystalline or amorphized samples, and at different temperatures, heating or cooling the sample with a liquid nitrogen-thermo resistance temperature controlled stage. We observed that an anomalous redistribution of boron occurs during the analysis of c-Si at RT, consisting in long tails on both the trailing and leading edges of the B deltas at concentrations below 1x1018/cm3. The phenomenon reduces significantly after amorphization or by cooling the sample, and it has been interpreted as the result of the interaction of substitutional boron with the I's injected in the samples by the sputtering beam. The profiles have been simulated and, as a result, the first experimental estimation of the B diffusivity at RT is provided. Such phenomenon has not been evidenced and discussed before, but it appears to be present in most of the B delta profiles shown in literature so far. As a consequence, many of the observations obtained in the past might be revised. Our data give significant insights on the migration and interaction of boron and point defects at RT and below.

12.50 **LUNCH**