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June 18 - 21, 2002

SYMPOSIUM O

The 300 mm Silicon Era: Material, Equipment, Technology

Symposium Organizers:

Hans Richter, IHP, Frankfurt(Oder), Germany

Masataka Umeno, Osaka University, Suita, Japan

Peter Wagner, Wacker Siltronic AG, Burghausen, Germany

Papers will be published in Materials Science in Semiconductor Processing

E-MRS 2002 SPRING MEETING

SYMPOSIUM O

Wednesday, June 19, 2002 — Afternoon
Mercredi 19 juin 2002 — Après-midi

SESSION I: 300 mm Roadmaps
Chairpersons: H. Richter (IHP) – M. Umeno (Osaka University)

14:00 **O-I.1**

A ROADMAP TOWARDS COST EFFICIENT 300 MM EQUIPMENT
P. Kuecher, Infineon Technologies SC300, Dresden, Germany, and L. Pfitzner, Fraunhofer-IISB, Erlangen, Germany

14:30 **O-I.2**

FROM OVERALL EQUIPMENT EFFECTIVENESS (OEE) TO OVERALL FAB EFFICIENCY (OFE)
H. Binder, E4 Technologies Schlieren, Switzerland and M & W Zander, Stuttgart, Germany, Th. Vonderstrass, M & W Zander, Stuttgart, Germany, and L. Pfitzner, Fraunhofer-IISB, Erlangen, Germany

15:00 **O-I.3**

FUTURE ROADBLOCKS AND SOLUTIONS IN SILICON TECHNOLOGY AS OUTLINED BY THE ITRS ROADMAP
W. Arden, Infineon Technologies, Munich, Germany

The International Technology Roadmap for Semiconductors (ITRS) is a joint global effort of the semiconductor industry and research community to define the future development and requirements of the semiconductor technology for the next 15 years. The paper will review the major challenges, potential roadblocks and proposed solutions for the industry as outlined in the ITRS 2001.

The major sections of the ITRS contain technical information about frontend processing and interconnect, device structures and memory concepts, lithography and metrology as well as factory integration and environmental issues. Specific emphasis is given to describe future requirements on new materials and material properties as well as topics related to silicon wafer sizes of 300mm and beyond.

Special issues will be addressed, for example new transistor gate materials, new solutions for interconnect beyond copper metals and low k dielectrics as well as new starting materials for wafer sizes beyond 300mm.

15:30 **BREAK**

SESSION II: Crystal Growth
Chairpersons: M. Umeno (Osaka University) – H. Richter (IHP)

16:00 **O-II.1**

DISLOCATION-FREE CZOCHRALSKI SILICON CRYSTAL GROWTH WITHOUT THE NECKING PROCESS
K. Hoshikawa, T. Taishi, Faculty of Education, Shinshu University, Nagano, Japan, and X. Huang, Silicon Technology Corp., Kitasaku-gun, Japan

In the growth of large size CZ-Si crystals, more than 300mm in diameter, the mechanical weakness of the thin neck formed during the necking process, which is essential for in dislocation-free Si crystal growth, may become problematic in the near future. We propose a new technique 1,2), which allows dislocation-free crystal growth without the Dash necking process 3) .

We have found that the dislocations due to thermal shock in the seed crystals do not generate if Si crystals heavily doped with B, In or Ge are used as seeds. It has also been found that lattice misfit at the interface between the seed and the grown crystal does not result in dislocations if the difference in concentration of the doping impurity between the two is below a certain value. These two results have made it possible to grow dislocation-free crystals without the necking process. Furthermore, we have been able to prepare seed crystals with any lattice constant by co-doping them with B and Ge, whose covalent radii are respectively smaller and larger than that of Si. The technique of using seed crystals co-doped with B and Ge for dislocation-free growth without the necking process can be applied to the growth of not only heavily doped Si for epitaxial substrates but also lightly doped or undoped Si for bulk substrates.

16:30 **O-II.2**

ACTIVE CONTROL OF MELT CONVECTION OF SILICON BY ELECTROMAGNETIC FORCE
K. Kakimoto, A. Tashiro, and T. Shinozaki, Research Institute of Applied Mechanics, Kasuga, Japan

This paper reports numerical investigation of oxygen transfer in silicon melt under a condition of Electromagnetic Czochralski (EMCZ), which was newly developed by Watanabe et al.[1]. Three-dimensional time-dependent flow of silicon melt was carried out under several types of cusp-shaped magnetic fields. We have also investigated how the relative position between the melt of silicon and the cusp-shaped magnetic fields affects oxygen transfer in the melt. Two types of electrodes in which electric current paths through from the crystal the electrodes were taken into account to investigate mechanism of heat and mass transfer in the melt. The calculation clarified that the electromagnetic force in azimuthal direction effectively suppressed natural convection due to centrifugal force. Moreover, it has been clarified that heat and oxygen transfer from a crucible wall to the solid-liquid interface was enhanced due to off-center of axially elongated vortex to the pulling axis. Furthermore, the relative position between the melt and the cusp-shaped magnetic fields plays an important role of oxygen transier due to inhomogeneous distribution of Lorenz force.

Ref. [1] M. Watanabe, et al, J. Crystal Growth, 193 (1998) 402.

16:50 **O-II.3**

APPLICATION OF ALTERNATING AND COMBINED MAGNETIC FIELDS IN THE 300 MM SINGLE CRYSTAL GROWTH

E. Tomzig, J. Virbulis, W. von Ammon, Wacker Siltronic AG, Burghausen, Germany, Y. Gelfgat, and L. Gorbunov, Institute of Physics, University of Latvia, Salapsis, Latvia

The increase of diameter in the silicon single crystal growth from 200 mm to 300 mm for industrial application, 400 mm or 450 mm for research respectively has triggered off the development of numerous new technologies, i.e. crystal growth supporting systems, low power hot zones, high strength of static magnetic fields, new quartzglas qualities. At WSAG new kinds of magnetic fields have been developed for 300mm CZ growth. In this paper, the results of alternating and combined magnetic fields are discussed. Instead of buoyancy driven convection, a magnetic field controlled melt flow has been obtained in the large melt volumina. The crucible wall temperature and, in turn, the quartzglas corrosion has been reduced. Furthermore the application of the magnetic fields allow the controll of oxygen in a wide range.

17:10 **O-II.4**

SILICON MELT CONVECTION IN LARGE SIZE CZ CRUCIBLES

J. Virbulis, Th. Wetzel, E. Tomzig, and W. von Ammon, Wacker Siltronic AG, Burghausen, Germany

The conversion to large silicon single crystals of 300 mm diameter requires larger crucibles with diameter of 28” and more. Corresponding batch sizes of more than 250 kg generate turbulent melt convection with large scale velocity and temperature fluctuations. Several efforts of the crystal growth industry are dedicated to the control of the interface shape and the related point defect distribution in the crystal, of the oxygen and particle transport, of the crucible overheating and of the conditions for dislocation free growth. Beside conventional means, steady and dynamic electromagnetic fields offer new possibilities to meet the continuously increasing demands for crystal quality and yield improvement. Numerical simulation helps to investigate the wide range of possible process conditions, to save a lot of experimental costs and to reduce time to market. Depending on the required accuracy and available computation resources, both two-dimensional (2D) or three-dimensional (3D) models are used. Typically, modifications of k-ε turbulence models are used for steady state 2D calculations. Large Eddy Simulation or Direct Numerical Simulation are used in 3D modeling. These models describe the heat and oxygen transfer in the near crystal region more accurate, however, the computational expenses increase drastically. Temperature measurements in the melt, carried out during the crystal growth and in model facilities, supply data for the verification of the numerical models, for direct process optimization and for a better understanding of the heat and mass transport behavior.

17:40 **O-II.5**

NUMERICAL MODELING OF POINT DEFECT CONCENTRATION IN CZOCHRALSKI SILICON CRYSTALS

M. Krause, J. Friedrich, and G. Müller, Fraunhofer Institute for Integrated Circuits, Erlangen, Germany

As miniaturization of semiconductor devices is progressing further, the dimension of the structures reaches the same order of magnitude as the size of voids (about 100 nm). As these microdefects have a negative impact on the yield of the production process, a low density of microdefects is an important requirement for the crystal quality. The ability of controlling point defects, which are a major origin for the generation of microdefects, during silicon growth is already of significance, but will even become more important in the future.

Numerical simulation is a valuable tool in the process of designing new geometries for crystal growth furnaces. It allows for testing several versions without causing a lot of experimental effort. In this paper the combination of the software package CrysVUn with a model for the calculation of point defect distributions is presented. This model takes into account diffusive and convective transport of the defects as well as the recombination process. By this means global modeling of the complete furnace and its impact on point defect distribution is possible.

CrysVUn together with the point defect model is applied to a virtual puller for growing Si crystals with 300 mm diameter in order to demonstrate, how different geometry variations can influence the thermal field in the crystal on the one hand and the density of self-interstitials and vacancies on the other hand.

18:00 **O-II.6**

PREDICTION OF BULK DEFECTS IN CZ SI CRYSTALS USING 3D UNSTEADY CALCULATIONS OF MELT CONVECTION

V.V. Kalaev, D.P. Lukanin, V.A. Zabelin, Soft-Impact Ltd., St. Petersburg, Russia, Yu.N. Makarov, STR GmbH, Erlangen, Germany, J. Virbulis, E. Dornberger, and W. von Ammon, Wacker Siltronic AG, Burghausen, Germany

The transition to 300 mm diameter in CZ Si crystal growth results in new requirements to crystal quality. Numerical simulation of crystal pulling process has become a very useful tool in the optimization of the crystal growth.

An advanced 3D unsteady model of the near melt zone of the Czochralski growth system (the crystal, melt, quartz crucible, and graphite crucible), combined with a 2D model of global heat and mass transport in the entire growth chamber has been developed. This approach allows us to overcome the limitations of the conventional 2D steady-state models and to improve significantly accuracy of the prediction of the melt flow and heat transfer. An engineering model of defect incorporation and clusterization in growing crystals has been developed. This model utilizes the results obtained with the combined 2D/3D model: the shape of the melt/crystal interface, temperature and oxygen distribution in the crystal. The model of bulk defect formation consists of two parts: first, initial defect incorporation is calculated within a 2D approximation, and, second, the clusterization of voids and oxygen precipitation is simulated.

Our computational model has been validated using experimental data on temperature fluctuations in the melt and oxygen level in the crystal. It is demonstrated that accurate prediction of the melt/crystal interface geometry, obtained using the 3D calculations, is critical for the prediction of defect characteristics of the crystal.

Thursday, June 20, 2002 Morning
Jeudi 20 juin 2002 Matin

SESSION III: Advanced Silicon Wafer 1
Chairpersons: V.V. Voronkov (MEMC Electronic Materials) - K. Hoshikawa (Shinshu University)

09:00 **O-III.1**
DOUBLESIDE POLISHING - A TECHNOLOGY MANDATORY FOR 300 MM WAFER MANUFACTURING
G. Wenski, Wacker Siltronic AG, Burghausen, Germany

09:30 **O-III.2**
DEFECT REQUIREMENTS FOR ADVANCED 300 MM DRAM SUBSTRATES
C. Kupfer, and H. Dietrich, Infineon Technologies, Munich, Germany

09:50 **O-III.3**
THERMODYNAMIC ANALYSIS ON THE DISTRIBUTION COEFFICIENT OF IMPURITIES IN CZOCHRALSKI SILICON
N. Inoue, H. Harada, RIAST, Osaka Prefecture University, Sakai, Japan, S. Uda, Electronic Device R&D Center, Mitsubishi Materials, and I. Ohkubo, RIAST, Osaka Prefecture University, Sakai, Japan

Doping control is a key technology in Czochralski silicon crystal growth. There have been no theoretical analyses on the distribution coefficient for CZ Si growth which successfully explain the most impurities, especially nitrogen. We have compared the reported distribution coefficients k and the solid solubility at the melting point Cs of most impurities and found the linear relationship. Most impurities data lie on the formula of Log k = Log Cs + M, where M denotes the constant depending on the impurity groups, such as donor/ acceptor dopants (column III and column V elements), column IV elements and light elements (C, N and O). Unlike the previous theories, this formula covers most elements. Moreover, this formula was deduced from the thermodynamic analysis. M was found to correspond to the melting temperature of the solutions, nearly equal to that for pure Si in case of light elements, a few degrees lower in the case of dopants and considerably lower in case of column IV elements. This result agrees well with the actual meting point reduction, because solution is dilute for light element whereas dense in case of column IV elements. This work is partially supported by the JSPS.

10:10 **O-III.4**
EFFECT OF VACANCIES ON NUCLEATION OF OXIDE PRECIPITATES IN SILICON
V.V. Voronkov, MEMC Electronic Materials, Merano BZ, Italy, and R. Falster, MEMC Electronic Materials, Novara, Italy

The use of installed, tailored vacancy concentration profiles (MDZ®) to precisely control oxygen precipitation behavior in silicon wafers has become an important technology for the 300 mm era. The advantages of such a wafer system are manifold. This paper presents a new model of one of the central physical processes important to the MDZ® system, that of the role played by vacancies to control the nucleation of oxygen precipitates. Steady-state nucleation of oxide precipitates is described by the distribution function *C*(*m*,*n*) over two basic size variables of an oxygen cluster: the number *n* of agglomerated oxygen atoms, and the number *m* of silicon atoms removed from the cluster location by vacancy consumption and self-interstitial emission.

The model is used to treat the experimental data of precipitation in wafers with controlled vacancy concentration induced by Rapid Thermal Annealing. The observed dependence of the precipitate density produced after 800^{o}C nucleation anneal (and measured after a final anneal at 1000^{o}C) on vacancy and oxygen concentration is well reproduced by the model, using the specific surface energy σ as a fitting parameter. The best-fit value was found to be approximately 900 erg/cm^2. The other fitting parameter, the number of self-interstitials emitted by the growing precipitates, per one oxygen atom, was found to be remarkably low, about 0.05.

10:30 **O-III.5**
OXYGEN PRECIPITATES IN 300 MM CZ-SI WAFERS
V.D. Akhmetov*, H. Richter*, IHP, Frankfurt (Oder), Germany, O. Lysytskiy*, BTU Cottbus, Cottbus, Germany, T. Müller, and R. Wahlich, Wacker Siltronic, AG, Burghausen, Germany
*Also: IHP/BTU Joint Lab, Cottbus, Germany

SESSION IV: Advanced Silicon Wafer 2
Chairpersons: K. Hoshikawa (Shinshu University) - V.V. Voronkov (MEMC Electronic Materials),

10:50 **O-IV.1**
ANALYSIS OF LOCALISED VIBRATION OF NITROGEN COMPLEXES IN CZ SILICON
I. Ohkubo, H. Harada, T. Mikayama, D. Funao, and N. Inoue, RIAST, Osaka Prefecture University, Sakai, Japan

Nitrogen doping reduces secondary defects in CZ silicon. It is necessary to establish the infrared measurement method of nitrogen (N) and nitrogen-oxygen (N-O)/point defect (N-V) complex concentrations. In this study, we examine the vibration of N-O and N-V complexes by the molecular orbital calculation. First, we analyze the N2O and N2O2 which are included in as-grown crystal. The structures used for calculation are Si40N2O(or O2)H54. Vibration mode and induced dipole moment by localized vibration are obtained by vibrational calculation. We have shown that the sum of absorption of N and N-O peaks is closely related to the total N concentration measured by SIMS. It is to be noted that oscillator strength is proportional to square induced-dipole. Weighted sum of absorption coefficient inversely proportional to oscillator strength is used in determining the conversion coefficient to N concentration. Next, we calculate the frequency and dipole moment of normal vibration modes of N2V and N2V2 which are formed and affecting the defect formation at high temperature. The structure used to calculate is Si34N2H36 and Si42N2H42. H2O-type and BF3-type asymmetric stretch vibrations were obtained. The frequency of N2V is 940cm-1 in H2O-type and 867cm-1 in BF3-type. 909cm-1 and 920cm-1 were obtained in N2V2 corresponding to H2O-type and the BF3-type vibration, respectively. We are trying to find these peaks experimentally. This work is partially supported by the JSPS.

11:10 **O-IV.2**
MECHANICAL PROPERTIES OF NITROGEN-DOPED SILICON SINGLE CRYSTALS
V. Orlov*, Institute of Solid State Physics of RAS, 142432 Chernogolovka, Moscow distr., Russia and BTU Cottbus, Germany, H. Richter*, A. Fischer, IHP, Frankfurt (Oder), Germany, J. Reif*, BTU, Cottbus, Germany, T. Müller, R. Wahlich, Wacker Siltronic AG, Burghausen, Germany,
*also IHP/BTU Joint Lab, Universitäts-platz 3-4, 03044 Cottbus, Germany

We report the results of our investigation of the effect of nitrogen doping level on plastic properties of 300-mm silicon material in the temperature range between 650°C and 1000°C. Undoped, low doped and highly doped materials were examined. The dependences of the upper and lower yield point and the dependence of the size of the dislocation rosettes, formed near the indentation, on temperature were obtained.

The experiments on the upper and lower yield point were carried out at two constant shear strain rates equal to $7\ 10^{-6}\ s^{-1}$ and $2.8\ 10^{-5}\ s^{-1}$. The indentation at elevated temperatures was performed in a specially made setup. A {110} surface was indented at temperatures between 500°C and 650°C in air.

An increase in the nitrogen concentration is shown to lead to enhanced upper and lower yield point. Possible mechanisms of interaction of dislocations with impurities resulting in hardening of silicon single crystals are discussed. FEM calculated data of bearing stress, coming up in vertically stacked 300-mm Si wafers, are compared with the upper yield point values obtained. The allowable process temperatures preventing plastic flow of Si wafers under load are significantly enhanced.

11:30 **BREAK**

11:50 **O-IV.3** DISLOCATION BEHAVIOR IN HEAVILY GERMANIUM-DOPED SILICON CRYSTAL

T. Taishi, Faculty of Education, Shinshu University, Nagano, Japan, X. Huang, Silicon Technology Corp., Kitasaku-gun, Japan, I. Yonenaga, Institute of Material Research, Tohoku University, Sendai, Japan, and K. Hoshikawa, Faculty of Education, Shinshu University, Nagano, Japan

We found previously that no dislocations form due to thermal shock in heavily B-doped Si seed during dipping in Si melt in Czochralski (CZ) Si crystal growth[1] and heavy B doping of Si crystal is very effective in suppressing dislocation formation[2]. In this study, we will present the dislocation behavior in heavily Ge-doped Si crystal.

Heavily Ge-doped Si crystals were grown by the CZ method using <001>-oriented Si seeds. Heavily Ge-doped Si seeds were cut from the grown crystals and used for growing Si crystals with the same Ge concentration as the seeds. The grown crystals were cut into wafers along their axial direction and examined by X-ray topography.

First, dislocation behavior due to thermal shock in Si seeds was investigated. Many dislocations were observed in an undoped Si seed, however no dislocations were observed in heavily Ge-doped Si seed when the Ge concentration in the seed exceeded 9x1019 atoms/cm3. Next, slip behavior in the bottom of Si crystal intentionally removed from Si melt was investigated. The formation of slips and the typical length of the slips in the heavily Ge-doped Si crystal was less than that in the undoped one. We, therefore, conclude that heavily Ge- doped Si crystal is very effective in suppressing dislocation formation, like heavily B-doped crystal.

[1] T. Taishi et. al, Jpn. J. Appl. Phys., 39, L191, (2000).
[2] I. Yonenaga et. al., J. Appl. Phys., 89, 5788, (2000).

12:10 **O-IV.4** DIFFUSION DOPING OF 300 mm SILICON PLATES BY MEANS OF SOLID PLANAR SOURCES OF BORON AND PHOSPHORUS

V.O. Voronin, Y.M. Bogdanovski, L.Z. Hasko, and V.M. Myshchyshin, Electrophysical Dpt., National University "Lviv Polytechnic", Lviv, Ukraine

One of methods for highly uniformly doping of large diameter 300 mm silicon plates is using of solid planar diffusion sources (SDS) of boron and phosphorus [1]. We analyzed conditions for statement of equilibrium concentration of gaseous doping agent near the surface of silicon plates at 4-12 mm distance between sources and silicon wafer in 800-1100°C temperature interval.

Uniformity of doping has been achieved at providing conditions of diffusion character for mass transfer of doping agent to silicon surface. Equilibrium concentration of doping agent are stated on all silicon surface during 0.1-30 sec after achievement of even temperature in reaction zone. Dispersion of surface resistance on 300 mm silicon wafer does not exceed ± 2 %.

12:30 **LUNCH**

Thursday, June 20, 2002 Afternoon
Jeudi 20 juin 2002 Après-midi

SESSION V: New Processes and Materials 1

Chairpersons: L. Pfitzner (FhG-IIS) – A. Schüppen (AIXTRON AG)

14:00 **O-V.1**

THE INVEST PROJECT: MBE FOR ADVANCED OXIDE EPITAXY

J.-P. Locquet, H. Siegwart, IBM Reseach, Rueschlikon, Switzerland, J.W. Seo, IPMC, Lausanne, Switzerland, J. Fompeyrine, IBM Reseach, Rueschlikon, Switzerland, A. Dimoulas, National Center for Scientific Research "Demokritos", Athens, Greece, P.-A. Nutte, F. Pruvost, and C. Chaix, RIBER SA, Rueil-Malmaison, France

The need for "new" materials in the semiconductor industry is so wide that the introduction of unusual steps in CMOS processes is likely. Alternate gate dielectric oxides are a clear example where atomic level control is required and induced interest for alternative deposition techniques like ALCVD or MBE. We will first present the EU consortium "INVEST", whose goal is to develop epitaxial gate dielectrics, using a specifically designed oxide MBE 8" tool. The materials issues will be listed, and we will put them in perspective with related points specific to the used oxide MBE processes. Practical examples will be given to illustrate the feasability of our approach.

14:20 **O-V.2**

THE 300 MM TRICENT® CLUSTER TOOL FOR SiGe, METALS, HIGH K- AND ORGANIC-MATERIALS: HETEROWAFER® TECHNOLOGY

A. Schueppen, M. Schumacher, F. Wischmeyer, C. Lohe, G. Strauch, and H. Juergensen, AIXTRON AG, Aachen, Germany

The most recent results from the new Tricent® 300 mm CVD/Epireactor platform for the deposition of mono and poly-Si, SiGe, SiGe:C, high k-materials ferroelectrics, and organic materials for OLED's are presented. Based on comprehensive CFD process and chamber simulation, the showerhead LPCVD reactor provides a couple of new features in comparison to standard CVD machines, i.e. a new thermostated showerhead, a flexible susceptor technique for various wafer sizes, temperature control by pyrometry / telemetry, and a state-of-the-art data logging system. The Tricent® cluster tool consists of a fully automated bulkhead mount handler for up to 4 Tricent® moduls, and / or RTA, and / or RTP cleaning modules. Based on the HeteroWafer® technology, process evaluations on SiGe, BST, STO, PZT and Pt reveal the extremely high level of control of the deposition process in this fully boundary-condition-controlled chamber for different semiconductor and optical applications.

14:40 **O-V.3**

SIGE AND SIGE:C EPITAXIAL PROCESS RESULTS FOR HBT APPLICATIONS ON 200 AND 300 MM WAFERS

B. Tillack, Y. Yamamoto, IHP, Frankfurt (Oder), Germany, J. Italiano, and H. Jia, ASM America Inc., Phoenix, USA

The paper presents process results of 200 mm and 300 mm SiGe and SiGe:C epitaxy deposited by Reduced Pressure CVD (RPCVD) in commercial single wafer systems (ASM Epsilon E2000 and E3000). Excellent uniformity is demonstrated as well for 300 mm SiGe as for SiGe:C. The prevention of B outdiffusion which is the main advantage of introducing C into the base of SiGe Heterojunction Bipolar Transistors (HBTs) is demonstrated using material and device data. Results showing a gain in HBT performance, a wider latitude in HBT process margins, and improved scalability of the transistors are presented.

The results demonstrate the excellent capability of the used RPCVD epitaxy process and tool for the SiGe:C HBT technology.

15:10 **O-V.4**

NANOTOPOGRAPHY OF SILICON WAFERS AND POST-CMP OXIDE THICKNESS VARIATION

R. Schmolke, R. Pech, H. Schwenk, Wacker Siltronic AG, Munich, Germany, R. Deters, P. Thieme, Infineon Technologies AG, Munich, Germany, and G. Diakourakis, ADE International GmbH, Kirchheim-Heimstetten, Germany

The impact of nanotopography of silicon wafers on the thickness homogeneity of oxide layers after deposition and chemo-mechanical polishing (CMP) is investigated. Comparison of nanotopographical height with post-CMP oxide thickness for the same position on a wafer may result in data with no obvious correlation. However, a simple relation is obtained when (i) the root-mean square roughness of nanotopographical height (sNH), (ii) the standard deviation of post-CMP oxide thickness in total (sOTD) and (iii) as caused only by fluctuations of the combination of oxide deposition and CMP (sCMP) are considered: $\sigma_{OTD}{}^2 = \sigma_{CMP}{}^2 + \alpha(\lambda_P)^2 \cdot \sigma_{NH}{}^2$. $\alpha(\lambda_P)$ is a coefficient that turns out to be fairly independent of the nanotopography of wafers but is essentially a function of the CMP planarization length λ_P. Regarding the CMP process used in our investigation, $\alpha \approx -0.15 \pm 0.05$, indicating that only 15% of the nanotopographical height values of as-polished wafers transfer into oxide thickness variations after CMP. Data and λ_P as presented in [1] allow to determine $\alpha(\lambda_P)$ more generally: $\alpha(\lambda_P) \approx 0$ for $\lambda_P < 1$ mm, $\alpha(\lambda_P) \approx [-0.09/\mathrm{mm}] \cdot \lambda_P + 0.12$ ($r^2 = 0.96$) for 1.4 mm $< \lambda_P <$ 12.4 mm and $\alpha(\lambda_P) \approx -1$ for $\lambda_P >$ 12.4 mm.

[1] D. Boning et al., Int. CMP Symp., Dec 4th 2000, CMP Total Solutions, Tokyo, Japan.

15:30 **O-V.6**

LINEARLY EXTENDED INDUCTIVELY COUPLED PLASMA (ICP) SOURCES FOR LARGE AREA FPD ETCH PROCESS APPLICATIONS

Y.J. Lee, K.N. Kim, B.K. Song, Dept. of Materials Engineering, Sungkyunkwan University, Suwon, Korea, J.K. Lee, and G.Y. Yeom, Dept. of Electrical Engineering, POSTEC, Pohang, Korea

In order to achieve the performance required for high resolution flat panel display (FPD) devices, especially for TFT-LCD of next generation, improved dry etch processes currently indispensable technology for semiconductor industry are required for volume manufacturing and superior critical dimension control. In this study, to improve both the plasma density and the uniformity of ICP source, several internal-type linear antenna designs have been used in a square shaped (830mm´1,020mm) plasma chamber to generate inductively coupled plasmas. A simple modeling and simulation with a 2-D fluid code were used to analyze the optimum arrangement and the distance of the each line source. The simple modeling analysis revealed that optimum distance of the each line sources existed for our internal-type linear ICP source. In this presentation, the effects of various arrangements of the linear antennas and process conditions on the plasma characteristics were investigated using a quadrupole masss spectrometer (QMS: Hidern Analytical Inc., PSM 500) and a Langmuir probe (Hiden Analytical Inc., ESP) located on the sidewall of the chamber. Also, the analyzed simulation data of the plasma parameters, such as plasma density, electron temperature, and plasma uniformity in this large area plasma source were compared with the experimentally measured data.

15:50 **BREAK**

SESSION VI: New Processes and Materials 2
Chairpersons: A. Schüppen (AIXTRON AG) – L. Pfitzner (FhG-IIS)

16:10 **O-VI.1**

NEW CHALLENGES FOR 300 mm Si TECHNOLOGY: 3D INTERCONNECTS AT WAFER SCALE BY ALIGNED WAFER BONDING

V. Dragoi, P. Lindner, M. Tischler, and Ch. Schaefer, EV Group E. Thallner GmbH, St. Florian, Austria

Wafer-to-wafer alignment and subsequent bonding are key enabling process steps for 3D interconnection of wafers through stacking. Device stacking is justified by the potential benefits attainable: size reduction, signal time delay reduction, decrease in power consumption, increase in speed and in device density, and extension of bandwidth. Unlike MEMS wafers that usually involve double sided processing, IC and CMOS wafers are always processed on a single side. Therefore wafer to wafer alignment must use alignment targets situated in the bond interface. In this paper we describe an original alignment procedure which can be applied for wafers up to 300 mm diameter: the SmartView® alignment system achieves micron alignment tolerances using a face-to-face alignment method, thus potentially eliminating extra processing steps, such as definition of back side alignment keys. The SmartView® system uses for alignment keys visualization two pairs of top-bottom microscopes located on the same optical axis. Wafer alignment uses encoded stage motors allowing fine X and Y movements (0.1 µm steps) and a small axis of Z-travel controlled by three software compensated independent spindle motors. The repeatability of the measurement system is <0.35 µm. Interconnects can be formed using deep etched vias in one wafer. After wafer bonding and subsequent thinning, the vias become accessible from the topside and the process can be repeated, in order to obtained a multiple-stack structure.

16:30 **O-VI.2**

THE Pr_2O_3/Si(001) INTERFACE: A MIXED Si-Pr OXIDE

D. Schmeißer, BTU Cottbus, Cottbus, Germany, and H.-J. Müssig, IHP, Frankfurt (Oder), Germany

Pr_2O_3 is a candidate to replace SiO_2 as the gate dielectric material for sub-0.1 µm CMOS technology. In order to maintain a high-quality interface and channel mobility, it will be important to have no metal oxide or silicide phases present at or near the channel interface. We studied the Pr_2O_3/Si(001) interface by a non-destructive depth profiling using SR photoelectron spectroscopy. We find that there is no silicide formation at the interface. We conclude that a chemical reactive interface exists, consisting of a mixed Si-Pr-oxide such as $(PrO_2)x(SiO_2)_{1-x}$, typically in non-stoichiometric composition.

Pr_2O_3 films are prepared in-situ by electron beam evaporation of Pr_6O_{11} at a deposition rate of 0.1nm/min. During deposition, the Si(001) sample was kept at 600°C to enable the heteroepitaxial growth of Pr_2O_3 [1]. We report on the Pr3d, Pr4d, Si2p, and the valence band features of films prepared with a thickness up to 1nm. The Pr core levels show that there is a mixed PrO_2/ Pr_2O_3 phase. The Si2p emission indicates the formation of a Si^{+2} feature. The valence band is dominated by the Pr4d and Pr4f states. The latter causes a high density of states right at the valence band maximum. We find that the composition of the interface is not dependent on the film thickness. Even at lowest coverage, the characteristic Pr and Si features are developed.

[1] H.J. Osten et al., IEDM Technical Digest (2000) 653.

16:50 **O-VI.3**

PRASEODYMIUM OXIDE GROWTH ON SI(001) BY PULSED-LASER DEPOSITION

D. Wolfframm, M. Ratzke, and J. Reif, IHP/BTU Joint Lab, BTU Cottbus, Cottbus, Germany

Friday, June 21, 2002 — Morning
Vendredi 21 juin 2002 — Matin

SESSION VII: Diagnostics and Metrology 1
Chairpersons: P. Wagner (Wacker Siltronic AG) – S. Kawado (Rigaku Corp.)

08:30 **O-VII.1**

X-RAY CHARACTERIZATION OF CRYSTAL PERFECTION AND SURFACE CONTAMINATION IN LARGE-DIAMETER SILICON WAFERS

S. Kawado, Rigaku Corp., Akishima-shi, Japan

This paper reviews recent development of X-ray techniques, which cover laboratory experiments and synchrotron radiation (SR) applications, to detect crystal imperfections and surface contamination in 300-mm CZ-Si wafers. Though process-induced defects can be easily detected by a large-sized Lang camera, it is difficult to observe grown-in microdefects and slight impurity inhomogeneity, even the double crystal method is applied. SR plane-wave X-ray topography has overcome this difficulty except for observing void defects with the help of its high strain-sensitivity. However, it cannot be applied to 300-mm Si wafers because of their warpage. Recently, X-ray topography using a 300-mm-wide monochromatic beam has been employed for measuring the warpage of large-diameter wafers as well as inspecting surface damage caused by various steps of wafer-manufacturing.

Energy-dispersive (ED) TXRF using a rotating-anode X-ray generator is now widely used for detecting traces of metallic impurities on 300-mm Si wafer surfaces. The requirement of LSI miniaturization for low LLD has promoted the combination of the vapor-phase decomposition technique and the TXRF. SR-TXRF using an ED solid-state detector is effective for its nondestructive and low LLD feature. Furthermore, newly-developed wavelength-dispersive SR-TXRF has good energy resolution. The combined use of the laboratory and SR experiments leads to precise information about crystal perfection and surface contamination in large-diameter Si wafers.

09:00 **O-VII.2**

PHOTOELASTIC STRESS EVALUATION AND DEFECT MONITORING IN 300 MM WAFER MANUFACTURING

H.D. Geiler, M. Wagner, H. Karge, Jena Wave, Jena, Germany, M. Paulsen and R. Schmolke, Wacker Siltronic AG, Burghausen, Germany

09:30 **O-VII.3**

PHYSICAL FAILURE ANALYSIS IN SEMICONDUCTOR INDUSTRY - CHALLENGES OF THE COPPER INTERCONNECT PROCESS

E. Zschech, E. Langer, H.-J. Engelmann, and K. Dittmar, AMD Saxony Manufacturing GmbH Dresden, Dresden, Germany

10:00 **O-VII.4**

SURFACE AND INTERFACE PROPERTIES OF SILICON-ON-INSULATOR MATERIALS CHARACTERIZED BY THE NONCONTACT ELECTRICAL METHOD

S. Nakamura, D. Watanabe, A. En, M. Suhara, and T. Okumura, Tokyo Metropolitan University, Hachioji, Japan

A silicon-on-insulator (SOI) material is attracting much attention as an ideal substrate for the next-generation high-speed, low-power and highly integrated devices. As the thickness of the top-Si layer in the SOI materials is reduced, electric properties of the surface as well as the buried Si/SiO2 interfaces become crucial to the device performance. Particularly, the electrical characterization of the SOI materials has been of great interest in virtually every step during the processing of the SOI wafers and devices.

In this paper, we demonstrate that the Kelvin-probe method, in combination with surface photovoltage (SPV) measurements, is promising for the nondestructive electrical characterization of SOI materials. With the use of ultraviolet light source for the SPV measurement, very thin SOI layers like the SIMOX-SOI material can be characterized by using the proposed method. In addition, we investigate that the light-intensity dependence of the SPV gives data equivalent to familiar I-V characteristics of diodes. Thus, we call the proposed method the contactless I-V method. In order to characterize electric properties of the surface as well as the buried Si/SiO2 interfaces, temperature dependence of the contactless I-V characteristics is also measured and compared for three kinds of wafers: bulk Si, bonded SOI and SIMOX.

10:20 **BREAK**

SESSION VIII: Diagnostics and Metrology 2
Chairpersons: S. Kawado (Rigaku Corp.) – P. Wagner (Wacker Siltronic AG)

11:00 **O-VIII.1**

INFRARED ABSORPTION MEASUREMENT OF NITROGEN CONCENTRATION IN CZ-SI CRYSTAL

T. Matsumoto, D. Funao, Y. Yamanaka, and N. Inoue, RIAST, Osaka Prefecture University, Sakai, Japan

We have established the infrared measurement method of nitrogen concentration in CZ silicon using 10 mm thick samples, that is to sum the absorbance of 3 peaks at 963, 996 and 1018 cm^-1, corresponding to N interstitial pair (N2) and N2-O, N2-O2 complexes, respectively. In this paper we examined the method and detection limit for the case of more convenient 2 or 1 mm thick samples. Double side mirror finished 2 mm or 1 mm thick samples were cut from the neighbor of the 10 mm thick samples. It was important to stabilize the apparatus and reduce the noise. In addition, correction for thickness difference between the measurement sample and the reference (N-free) sample as well as elimination of oxygen absorption peaks around N-O peaks were crucial to delineate the small N-related peaks and obtain the absorbance accurately. It was able to detect the absorption peaks of samples whose N concentration was more than 5E+14 cm^-3 (absorbance around 1E-5). In some cases thickness interference fringes appeared and were eliminated. Good agreement was observed between the absorption coefficients of 10 mm thick samples and those of 2 or 1 mm thick samples. This work is partially supported by the JSPS.

11:20 **O-VIII.2**

IMPACT OF FILTERING ON NANOTOPOGRAPHY MEASUREMENT RESULTS OF 300 MM SILICON WAFERS

F. Riedel, and P. Wagner, Wacker Siltronic AG, Burghausen, Germany

The non-planar flatness deviation of the Si wafer front-surface within a spatial wavelength regime from about 0.5 to 20 mm is denoted as nanotopography (NT). Present 0.13 µm and future technology generations necessitate NT measurements especially to meet requirements of chemo-mechanical polishing process steps. Appropriate optical tools are capable measuring and mapping the surface with the sensitivity required. Long-wavelength contributions to the height map are eliminated by high-pass filtering in order to extract the NT features of interest. These are then characterized and discriminated by evaluating height variations of the filtered map within different analysis areas. In the present paper, the impact of various filter schemes used for NT measurement evaluation is reported. Height maps of wafers measured with an interferometric tool are processed with different filter settings in an experiment with factorial design. Filter cut-off wavelength, data extrapolation at the wafer edge, and NT metric are varied on two levels each. It turns out that the so-called Peak-to-Valley and Deviation metric correlate well. Long wavelength contributions dominate NT results, which is revealed by comparing long and short filter cut-off wavelengths, respectively. Data extrapolation beyond the wafer edge is necessary to avoid transient effects if a filter with finite width approaches the boundary of the fixed quality area, which results in an interaction between filter cut-off wavelength and data extrapolation technique used. Wafers with excellent NT exhibit little dependence on filtering scheme.

11:40 **O-VIII.3** METROLOGY SOLUTIONS FOR ULTRA THIN GATE DIALECTRICS AND OTHER THIN FILM APPLICATIONS, S. Bryan, Physical Electronics Inc., 6509 Flying Cloud Drive, Eden Praire, MN 55344, USA and W. Betz, Physical Electronics GmbH, Fraunhoferstrasse 4, 85737 Ismaning, Germany

The characterisation and control of nitrided Si oxides, which are being used as the gate oxide for next generation high performance semiconductor devices, is critical for process development and manufacturing. These thin SiON films overcome the high leakage current and B diffusion inherent in ultra-thin SiO$_2$. However, the resulting device performance is very dependent on the N distribution, the total N dose and the film thickness. Thus, analytical techniques, such as XPS and TOF-SIMS that can readily characterise the variation in the N distribution for different tools and processes, play an important role in the development and ramp-up of the gate process. Additionally, in order to optimise the process window and to control the manufacturing of an SiON film, it is necessary to routinely monitor the N dose and the film thickness. Specially designed XPS surface measurements provide a non-destructive and direct measure of N dose and film thickness, with high precision that is unaffected by molecular airborne contamination. These measurements are shown to be sensitive to changes in N dose and oxide thickness.

Device performance and integrity is highly sensitive to surface metal contamination prior to gate oxide. The most recent *ITRS* has reduced the critical surface metals for Na, K, Ca, Co, Cu, Cr, Fe, Mo, Mn and Ni to < 9x10^8 atoms/cm^2. This is at or below the detection limit for TXRF. TOF-SIMS, on the other hand, is well suited for this application, with detection limits well below those of TXRF. The move of the semiconductor industry to copper (Cu) interconnect lines has created a real need for Cu contamination monitoring and control. The ability of TOF-SIMS to quantify Cu levels on patterned wafers provides a crucial capability for new Cu metallization technologies. Examples of the detection limits and measurement approaches for TOF-SIMS will be given.

12:00 **O-VIII.4** MEASURING THE DIMENSIONS OF CONTOURS ON IMAGES OF SILICON MATERIALS
A. Borisenko, and Y. Zuban, Sumy State University, Ukraine

When measuring the geometry dimensions on images of silicon materials there are tasks, related to determination, for example, diameters of rings, arch curvature, distance apart the points and others. A lot of images are referable to certain class and information about this class can be used for more effective image analysis. The offered method of local windows for image analysis is based on such an approach.

Local windows are formed using electronic system. They represent the template of contours of a image class. This template is matched on the image of the sample. Affiliation to the chosen class is defined by analyzing a zone of the image in the local window. Using automatic fitting the most relevant template it is given the information about geometry parameters of analyzing image contour with a specified degree of accuracy. It is possible to define desired value with greater degree of accuracy within chosen template using auxiliary analysis the zone of image in local window, if it is necessity.

The method of local windows allows to realize the algorithm, described above, as electronic device, which is integrated with measurement equipment, for example microscope. This method allows to perform high-precision analysis of geometry dimensions of contours on images of silicon materials.

12:20 Closing Remarks: P. Wagner